# Research on Electromagnetic Interference of DC / DC Converter

Hou Junrui, Li Pengfei, Chen jing, Wang Fude, Yuan Guifang

Beijing Research Institute of Precise Mechanics and Controls

Beijing china

houjunr@163.com

***Abstract*—In this paper, the low voltage and high current driver is used as an example to analyze and suppress the EMC problem caused by DC / DC power conversion. In the process of low-voltage and high-current driver design, the problem of misalignment of the drive signal occurs. The paper analyzes the mechanism of the electromagnetic interference in the switch process, and then detects the electromagnetic interference caused by the frequency conversion system. Proposed an improved method, and carried out experimental verification, and finally achieved a better use effect.**

***Keywords—electric vehicle driver; DC/DC power conversion; Electromagnetic compatibility***

## I. INTRODUCTION

During the design of the low voltage and high current driver [1], the upper (upper) tube gate drive signal oscillates during the opening of the upper (lower) tube of the same bridge when the bridge inverting circuit is driven. Oscillation when relatively large, will switch the device conduction, resulting in power switch device through and damage[2].There are a variety of reasons for misleading, such as improper design of DC/DC power supply structure[3], improper selection of MOSFET[4], poor circuits design[5], serious electromagnetic interference[6], etc. This paper analyzes the electromagnetic interference generation mechanism of DC/DC converter of driver. Based on the analysis of the EMI generation mechanism of the DC / DC converter, the EMI of the DC / DC converter is seriously affected, which affects the conduction of the switch tube and lead to the excessive testing of the EMI regulations. This paper presents a method to optimize the design, and through experiments to verify the similar problem of interference.

## II. CIRCUIT STRUCTURE AND INTERFERENCE FORMATION MECHANISM

### *A. The circuit structure and working principle of DC/DC converter*

Under normal circumstances, DC / DC power conversion in the drive design, must be transformed several times to provide power supply voltage for multiple electronic components, the conversion of the power supply often provide power for the half-bridge driver, transistor, control circuit chip, Flyback power supply and other circuits. Therefore, there are multiple sets of power transformations on the secondary side. As shown in Fig.1.

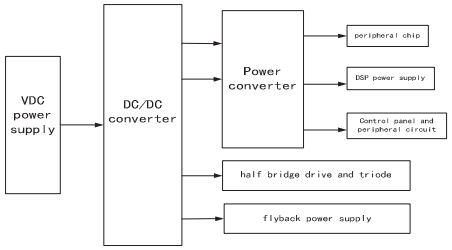


Fig. 1. DC / DC converter structure

### *B. DC / DC Transformer Conduction Coupling Mechanism*

Without considering the influence of the working current signal and leakage inductance on the electromagnetic interference propagation model, the DC / DC transformer interference propagation analysis model is established. Assume that the electromagnetic interference current flowing from the primary side of the high frequency transformer is $I_n$ ,The current part $I_{ci} = (i = 1, 2, ....., n)$ of the current through the primary and secondary coupling capacitor flows to the transformer secondary, the other part $I'_n$ of the current flow back to the primary side, taking into account the impact of distributed parameters[3].

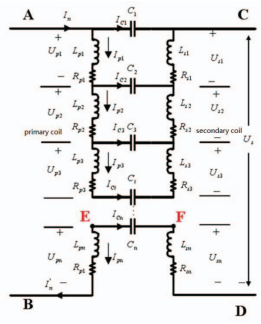


Fig. 2. High-frequency transformer interference propagation path analysis model.

The primary winding and the secondary winding of the transformer are divided into n segments according to the axis of the winding (the larger the n is, the closer the distribution parameter is to the actual state), and then n segments winding in series connected by inductance and resistance are formed, The secondary side is the same as the primary side. The

distributed capacitance is also considered as N parts only when the adjacent primary winding is considered [7].

$$L_{p1} = L_{p2} = ... = L_{pn} = \frac{1}{n} L_p \tag{1}$$

$$C_1 = C_2 = ... = C_n = \frac{1}{n} C_{PS} \tag{2}$$

$L_p$ :Each inductor is 1/n of primary inductance

$R_p$ :Each section of the resistor is 1/n of primary winding

$C_i$ :Each distribution capacitance

$C_{ps}$ : 1/n of the total capacitance,

In this way, the primary side current $\dot{I}_n$ can be expressed as:

$$\dot{I}_n = \dot{I}'_n + \dot{I}_{c1} + \dot{I}_{c2} + ... + \dot{I}_{cn} \tag{3}$$

The primary side winding voltage is:

$$\dot{U}_{pi} = \dot{I}_{pi} \bullet \dot{Z}_{pi} = \dot{I}_{pi} \bullet (R_{pi} + j\omega L_{pi}) \tag{4}$$

For the primary side of the winding voltage (4) sum can be obtained at both ends of the primary winding EMI voltage:

$$\begin{aligned} \dot{U}_p &= \dot{U}_{p1} + \dot{U}_{p2} + ... + \dot{U}_{pi} + ... + \dot{U}_{pn} \\ &= \dot{I}_{p1} \bullet \dot{Z}_{p1} + \dot{I}_{p2} \bullet \dot{Z}_{p2} + ... + \dot{I}_{pi} \bullet \dot{Z}_{pi} + ... + \dot{I}_{pn} \bullet \dot{Z}_{pn} \\ &= \dot{I}_{p1} \bullet (R_{p1} + j\omega L_{p1}) + \dot{I}_{p2} \bullet (R_{p2} + j\omega L_{p2}) + ... \\ &+ \dot{I}_{pi} \bullet (R_{pi} + j\omega L_{pi}) + ... + \dot{I}_{pn} \bullet (R_{pn} + j\omega L_{pn}) \end{aligned} \tag{5}$$

The voltage $\dot{U}_{c1}$ across the primary capacitor $C_1$ of the transformer is:

$$\dot{U}_{c1} = \dot{I}_{c1} \bullet \dot{Z}_{c1} = \dot{I}_{c1} \bullet \frac{1}{j\omega C_1} \tag{6}$$

Similarly, with reference to (1.4), the voltage across the distributed capacitor $\dot{U}_{ci}$ is:

$$\dot{U}_{ci} = \dot{I}_{ci} \bullet \dot{Z}_{ci} = \dot{I}_{ci} \bullet \frac{1}{j\omega C_i} \tag{7}$$

As in (7), when the interference signal is coupled from the primary winding to the secondary winding, the parasitic capacitance (i.e., the distributed capacitance $C_i$ above) is raised. The distributed capacitance causes a voltage drop that causes the secondary voltage to be coupled to the secondary winding, from Fig.2,the F point potential is the difference between the potential voltage $\dot{U}_{cn}$ of the E point potential and the parasitic capacitance $C_n$ :

$$\begin{aligned} \dot{U}_{sn} &= \dot{U}_{pn} - \dot{U}_{cn} \\ &= \dot{I}_{pn} \bullet (R_{pn} + j\omega L_{pn}) - \dot{I}_{cn} \bullet \frac{1}{j\omega C_n} \end{aligned} \tag{8}$$

As in (8), when the interference signal is coupled from the primary winding to the secondary winding, the parasitic capacitance is raised, The distributed capacitance causes a voltage drop which causes the secondary voltage to be coupled to the secondary winding, The variation of the F point potential is the difference between the potential voltage of the E point potential and the parasitic capacitance, as shown in Fig. 2:

$$\begin{aligned} \dot{U}_{si} &= \dot{U}_{pi} - \dot{U}_{ci} \\ &= \dot{I}_{pi} \bullet (R_{pi} + j\omega L_{pi}) - \dot{I}_{ci} \bullet \frac{1}{j\omega C_i} \end{aligned} \tag{9}$$

Therefore, it is possible to obtain the interference voltage $\dot{U}_s$ to which the secondary ends are coupled:

$$\begin{aligned} \dot{U}_s = &\left[ \dot{I}_{p1} \bullet (R_{p1} + j\omega L_{p1}) - \dot{I}_{c1} \bullet \frac{1}{j\omega C_1} \right] + \\ &\left[ \dot{I}_{pi} \bullet (R_{pi} + j\omega L_{pi}) - \dot{I}_{ci} \bullet \frac{1}{j\omega C_i} \right] + ... + \\ &\left[ \dot{I}_{pn} \bullet (R_{pn} + j\omega L_{pn}) - \dot{I}_{cn} \bullet \frac{1}{j\omega C_n} \right] \end{aligned} \tag{10}$$

Theoretically, (10) is the size of the EMI signal from the primary winding through the capacitor to the secondary winding. As can be seen from the analysis (10), since the inductance and the resistance value of the primary winding are related to the number of turns and the diameter of the coil, it has been determined in the design of the transformer, and the space for optimization is very limited. Therefore, changing the size of the inter-stage distributed capacitance to suppress the effect. The design parameters shown in figure 3.

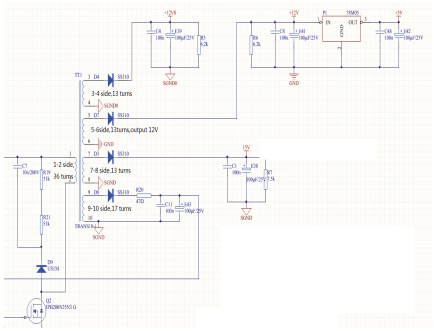

Fig. 3. DC/DC power converter PCB layout.

## III. ANALYSIS OF ELECTROMAGNETIC INTERFERENCE MECHANISM

DC / DC converter main circuit and drive circuit in the course of work will produce EMI. Some high-power switching

devices through the switch action format large pulse current and voltage. The rapid transient of voltage and current will produce radiation and noise, especially the rapid rectification of power electronic devices, motor starting, high-pressure radiation will cause higher field strength conduction and radiation harassment, which is the system to produce electromagnetic interference of the root causes. Through the DC / DC converter main circuit and PCB layout, we can see that the main interference source of the circuit from the MOSFET and the power diode, and PCB layout unreasonable is a huge cause of interference

### A. *MOSFET interference mechanism analysis*

MOSFET switch V is the core of the power converter and the most important source of interference. As an interference source, the interference signal generated by the MOSFET is mainly composed of two parts.

- The interference caused by the rising edge of the signal is related to the steepness of the signal.
- The interference caused by the distortion of the signal caused by stray capacitance or inductance.

V is connected with the high-frequency transformer, the load process is continuous, the following figure shows the MOSFET cell structure and its circuit model.

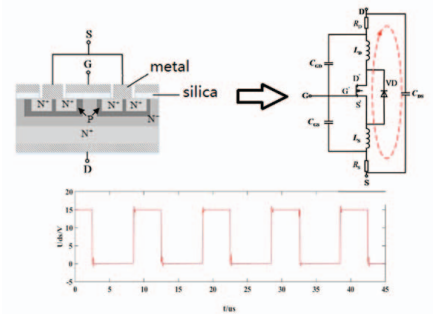


Fig. 4. MOSFET switching characteristics.

### B. *Interference Analysis of Power Diodes*

Converter connected with the coil of the four diodes(Fig.5) $D_1, D_2, D_3, D_4$, and diodes from the conduction into the cut off due to the examiner time is very short, prone to reverse current surge. The diode turns off the waveform as figure 5.Assume that the current flowing in the $D_1$ before time t1 is that the diode forward voltage is $\Delta U$ .At the time $t_1$, $D_1$ begins to turn off and the current flowing through the two stage begins to decrease, Then reverse and increase,

At the time $t_3$, $i_{D1}$ achieves a negative current peak, and Then the absolute value of $i_{D1}$ is reduced rapidly. The sudden change of $i_{D1}$ produces a very high inductive potential on the line inductance[6], which is applied to $Z_1$, the voltage pulse is generated. At the time $t_4$, the reverse recovery current of $D_1$ is reduced to zero. As the reverse recovery current quickly drops to zero, the $di/dt$ is great, the current flows through a circuit consisting of $L_1$, $D_1$ and an output capacitor C, The current loop will radiate high frequency electromagnetic waves to the surrounding space, interfering with sensitive components. As the DC output line there is distributed capacitance and inductance, high-frequency surge current flow through the high-frequency attenuation oscillation, the DC output to form differential mode interference.

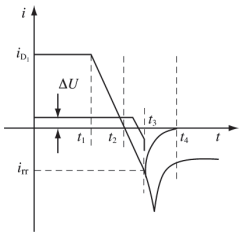


Fig. 5. Current and voltage waveform when the diode is turned off.

### C. *Tests and Analysis of Electromagnetic Interference Characteristics*

In this paper, a 10kW / 100V motor drive experiment platform is built to test the conduction interference and radiation interference of DC / DC converter in the state of 100A load current when the power battery is fully charged with 100V and DC / DC converter. Parameter settings refer to CISPR25 requirements. Figure 6 and 7 shows the experimental block diagram and platform

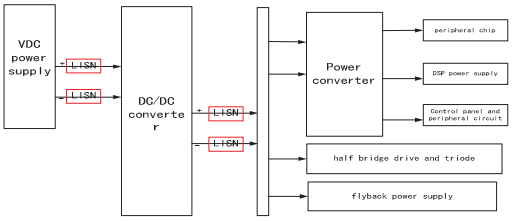


Fig. 6. the experimental block diagram

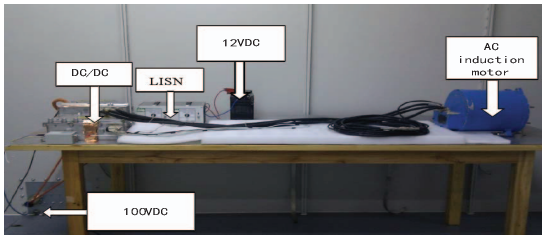


Fig. 7. the experimental platform.

The main reason for the system to generate electromagnetic interference is the fast power-off device, which includes the IGBTs in the high-voltage power loop of the converter, the MOSFETs and the crystal in the low-voltage control board DC-DC converter. The frequency of DC / DC and crystal is determined, and the frequency of interference is the operating frequency or its frequency, and the switching frequency varies with the modulation mode, and the interference frequency is wide and complex.

## IV. ELECTROMAGNETIC INTERFERENCE SUPPRESSION METHOD

### A. Optimize the drive circuit of the power switch

the design of the buffer absorption circuit can inhibit the switch V over-voltage and $du/dt$ or over-current and $di/dt$, while reducing the MOSFET switching losses. As figure 8shows, parallel capacitor buffer circuit can be used, the capacitor can change over-voltage electromagnetic energy into static energy to store, the resistor can prevent resonant between the capacitor and the circuit inductance. The capacitance and bus inductance is proportional, Design of double tinplate is used in Power bus, bus inductance significantly reduced, the value of Absorption capacitance can be reduced. In addition, select the appropriate drive circuit parameters, can maintain the circuit performance at the same time lower EM I level.

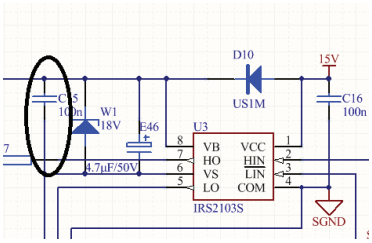


Fig. 8. PCB layout Parallel capacitor snobbier of drive circuit.

### B. Optimization of the PCB layout

DC / DC power converter in the PCB board placed improperly on the location will cause a huge EMI, the drive board can be designed for the four-tier board, the middle two layers for the power layer and formation, the top and bottom for the signal layer, Digital power and analog power lines, according to the function will be separated from the bottom layer to reduce the length of the alignment and the circuit area is the current length of the circuit to keep the minimum signal line and loop as close as possible.

### C. Optimization of drive Circuit for Power Switch

Add RC filter circuit In the drive signal transmission process, As figure 9 shows, the buffer absorption circuit design can inhibit the switch Z1 over voltage and $du/dt$ or over current and $di/dt$, while reducing the switching losses.

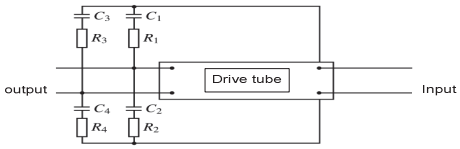


Fig. 9. RC filter circuit.

### D. Shielding and structural design

In addition to the main interference source inside the DC / DC converter, the PWM drive circuit and other control circuits are required to generate interference, in addition to high and low voltage through the formation of conductive interference, but also may radiate electromagnetic energy. Therefore, for the reduction of DC / DC radiation interference, the use of better thermal conductivity of the aluminum alloy shell to shield the internal interference source. Shielded shell using casting process, sealing cover for the gland, the direction of the force to maintain consistency. High-voltage input wiring harness with insulating sheath, enhanced sealing and safety performance.

### E. Experimental results

As in fig.10, The figure below shows the peak and mean test results of the 12V low-voltage output side of the DC / DC converter using the EMI optimization technique in the 90kHz-180MHz conduction EMI band (blue is the pre-optimization result, the red dotted line is optimized After the test results). It can be seen that the use of EMI optimization measures and DC / DC converter low-voltage output of the interference emission significantly reduced, EMC achieved performance requirements.

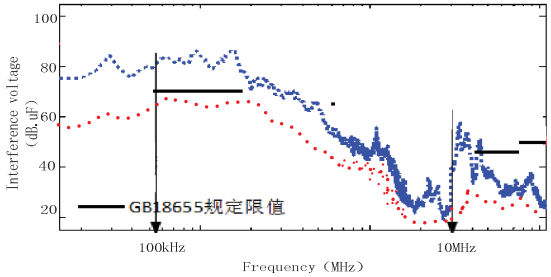


Fig. 10. Drive signal output before optimization.

## CONCLUSION

This paper analyzes the causes of the problems and analyzes the electromagnetic interference at different frequencies, and finally adjusts the structure of the DC / DC converter, drives the signal to add the filter, and then analyzes the causes of the problems caused by the misalignment of the drive signals encountered in the process of designing the electric vehicle. Capacitor, adjust the PCB layout to solve this problem.

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