# Practical Implementation of High Power and Efficiency Dc-dc Full-Bridge PWM Boost Converter

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*Abstract*—**Design and simulation problems of high power full-bridge boost converter with 175…320 VDC supply voltage are considered. The converter under investigation consists of a full-bridge inverter, a boost high-frequency transformer, a diode rectifier connected to a capacitive filter and an active load. Additional inductance, connected in series with the transformers primary winding, is brought in the converters structure to achieve soft commutation of power switches and limitation of the current switched by them, in order to improve the reliability of the device and increase its efficiency of energy conversion. Selection of the additional inductance value is an important task, because too much of it could not allow to provide load power requirements, and too small of it could bring about defects of expensive power semiconductor elements. The choice of additional inductance is also complicated by the difficulty of measuring the transformer leakage inductance with sufficient accuracy. This problem is solved using the proposed method of selection the additional inductance value, based on an analysis of the mathematical model and on an analytical description of the output inverter current curve. We also propose increasing of energy transformation efficiency by variation of the PWM carrier frequency. The curves that measured on real device 100 kW (175 ... 320V / 610V) show correctness of the model and the proposed method of selection of the carrier frequency and the additional inductance value.**

***Keywords—full-bridge inverter; boost converter; soft commutation; phase-shift control; transformer leakage inductance; variable carrier frequency.***

## I. INTRODUCTION

Power electronics development opens up prospects of energy converters design with high efficiency of semiconductor components usage and simultaneous improvement of weight-and-size indices of devices and cost reducing. But wide range of components, topologies and control schemes complicates the choice of an optimal topology of power cascade with reliable performance of the designed device. Simulation of impulse systems can solve this problem partly.

Scheme of full-bridge inverter with boost transformer is implemented for low input and high output voltage at high power and frequency. The advantage of this scheme compared to buck-boost converter is galvanic isolation, and compared to half-bridge is half the value of switching current. But introduction of transformer complicates the converter analysis due to its non-ideality: it is rather difficult to estimate with sufficient accuracy the value of the transformer leakage inductance which brings significant changes to performance characteristics of the bridge inverter. At the same time, for the chosen topology "soft" commutation of the power switches could be ensured: zero voltage switching (ZVS) mode of the power switches for full supply voltage range, and zero current switching (ZCS) for values closed to the minimum of supply voltage [1].

This type of converters is implemented in various industries, such as oil plants, marine power systems and widely applied frequency converters with DC input voltage. There are different approaches to improving the scheme topology of ZVS full-bridge converters by additional components introduction such as auxiliary inductances, diodes, serially connected transformers [2-8], but selection of these components and analysis of their characteristics requires time and increases the cost of the device.

In this paper we consider the full-bridge converter which topology consists of minimal quantity of elements and includes a full-bridge IGBT inverter, a boost transformer and a diode rectifier. The transformer leakage inductance value might not be enough for sot commutation mode ensuring and to limit the switching currents. In this case it is necessary to include additional inductance which can be connected both to primary and secondary transformer winding. Determination of the inductance value is a very important problem as its large values can lead to increasing of losses. Some researchers suggest determining its value from conditions based on unknown values: drain-to-source capacitance of MOSFET or collector-to-emitter capacitance of IGBT [6, 7, 10].

There are also might be difficult to determine leakage inductance of real transformer windings as its value depends on frequency, core design, mutual position of primary and secondary windings and number of turns. There are many approaches to determine these values [11-13] - either experimental or theoretical investigations. Experimental approaches require taking into account ratio of measuring device accuracy and the measured value. Theoretical approaches require knowledge of design parameters values, but some of them might be unknown.

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In [14] approaches to efficiency rise by PWM frequency variation are considered for the case when load varies in the range of 5-100%, and an adaptive control system realization is described in detail. In this paper analysis of the current curve is presented which allows determining frequency for different values of supply voltage.

In this paper an approach for selection of an additional inductance is proposed: maximum value is obtained by output inverter current curve analytical description taking into consideration variation of PWM frequency depending on input voltage.

The reminder of the paper is organized as follows. Section "Problem Statement" contains the converter functional diagram and its main characteristics. Also the problem of selection an additional inductance value is stated. A model and a simplified equivalent diagram of the investigated converter which allow analytical estimation of the additional inductance maximum value and PWC frequency calculation are received in section "Main Result". Section "Example" contains data from the real device with power 100 kW (input 175-320 VDC; output 610V/164 A) and a numerical example which confirms correctness of the model and proposed method of the additional inductance value selection.

## II. Problem Statement

Let us list the main parameters of the designed boost voltage converter: supply voltage is 175-320 V, rated supply voltage 250-280V, output stabilized voltage is 610 V. Maximum current switched by IGBT (two intelligent power modules are used PM800DV1B060 Mitsubishi Electric Semiconductor [15]) is 1250 A. Minimal output power is 100 kW. Parameters of the device power elements: transformer ratio is 1:6, capacitor bank capacity is 9900 μF, optimal commutation frequencies up to 10 kHz.

Converter considered in this paper consists of a full-bridge inverter loaded with power transformer which is connected to a rectifier. Such a system should maintain predetermined average voltage (610 V) on the output of diode rectifier and filter by feedback control. Output voltage should be constant despite the changes of the input voltage. Selected structure of the converter includes transformer leakage inductance which value is impossible to be determined exactly. This fact complicates the choice of the additional inductance.

Functional chart of the converter power part is shown in Fig.1. The following notations are used: *DC* is DC voltage source, *VT1-VT4* are IGBT transistors of the full-bridge inverter, *VD1-VD4* are diodes, *L* is additional inductivity, *T* is high frequency boost transformer, $C_f$ is a capacitive filter, $R_l$ is an active load resistance.

Let us state the problem of obtaining a computational model of the considered boost converter (see Fig.1) and output inverter current curve analytical description to determine the maximum value of additional inductance for the ensuring soft commutation mode and to limit switching current and optimize energy transformation.

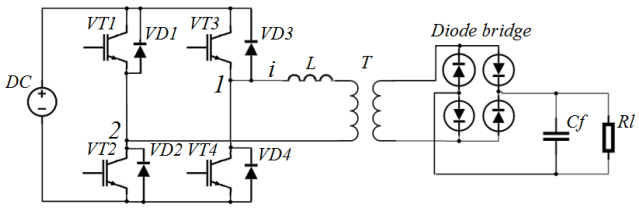


Figure 1. Functional chart of the converter

## III. Main Result

Consider model of the boost converter of 100 kW power with phase-shift switching algorithm of IGBT transistors.

The computational model of this system was created with Power Elements toolbox of Matlab Simulink and is shown in Fig. 2. This model includes the subsystem "Bridge Inverter" shown in Fig 3.

In Fig. 2 we use the following notations: $L$ is inductor of the primary winding of the transformer, $C_f$ is capacitive filter, $R_l$ is active load resistance (chosen as 3.6 Ω which matches 100 kW); transformer is given as "Linear Transformer" element with rated power, frequency and voltages of primary and secondary windings. Resistance of the primary circuit is set very small, not equal to zero; its leakage inductance is 1 μH. Resistance $R_m$ of the magnetizing circuit is set very large. Other windings parameters are set equal to zero. Value of the additional inductance is set approximately 3 μH.

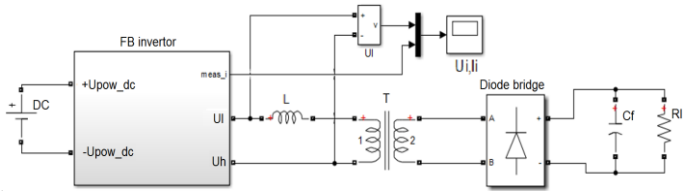


Figure 2. The computational model of the DC-DC converter.

Fig. 4 shows multipolar rectangular pulses of the inverter output voltage with the same duration $0.5T_{PWM}K_{PWM}$ and amplitude 230 V equal to inverter supply voltage, where $T_{PWM}$ is period of PWM carrier frequency, $K_{PWM}$ is PWM coefficient. Fig.4 also shows control signals *S1-S4* of the transistors *VT1-VT4* respectively. It also shows there is a time delay between transistors control signals which ensures soft commutation of switches [7], switching at zero voltage. Control signals *S3* and *S4* are shifted with respect to *S1* and S2 that is phase-shift control is realized and pre-assigned stabilized voltage on the converter output is obtained. Fig. 5 shows current and voltage (between nodes 1 and 2 in Fig.1) curves on the output of the full-bridge inverter, PWM frequency is 7.5 kHz.


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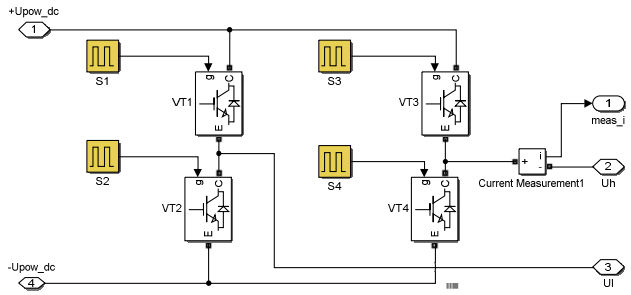


Figure 3. The subsystem "Bridge Inverter".

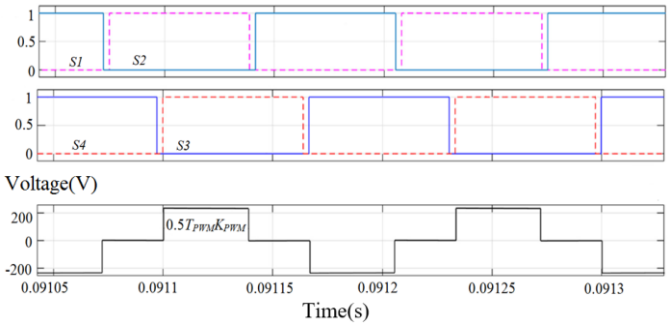


Figure 4. Control signals and output inverter voltage.

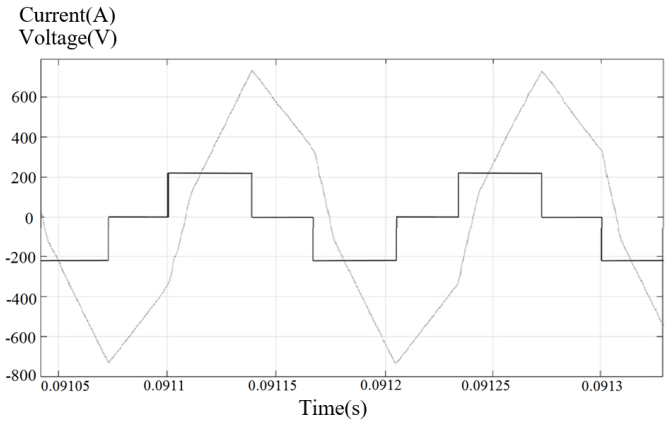


Figure 5. Output inverter current and voltage

Fig.5 illustrates the following transistors commutation law: transistors *VT1*, *VT4* are switched on the first specific current plot area (dashed lines in Fig.4). Current from supply source flows through transistor *VT1*, inductance and the transformer primary winding (let us suppose that polarity is positive) then trough transistor *VT4* to the supply source. Then *VT1* is switched off and *VT2* is switched on after time delay. During the time delay *VD2* conducts current. After switching on of *VT2* short circuit of transformer is retained (*VT2* and *VD2)*, the second specific current plot area appears and current may fall down to zero for small values of $K_{PWM}$. Then *VT4* is switched off, *VT3* is switched on after time delay, continuity of current in case it has not fallen to zero in ensured by diode *VD3*. Polarity of voltage of the inverter output is changed (*VT2*, *VT3* are on). If current has not fallen to zero it is conducted by *VD2*, *VD3*, and it flows into supply source. Simultaneously negative polarity current grows in the load by *VT2, VT3*. Total current will fall down faster until it goes through zero, after that it growth (negative polarity) slows. If current falls to zero before the transistors switching, then negative polarity current growth will be observed after the switching thanks to pair *VT2, VT3*. Then transients repeat with negative polarity current.

Consider the following substitution connection of the boost converter [16].

In Fig. 6 we use the following notations: *L, R* are inductance and resistance of the additional inductor; $L_1$, $R_1$ are leakage inductance and resistance of the primary transformer winding; $L_m$, $L_2$, $R_2$ are magnetizing, the secondary leakage inductance and winding resistance modified to the primary side; $C_f$, $R_l$ – capacitance bank capacity and load resistance modified to the primary side.

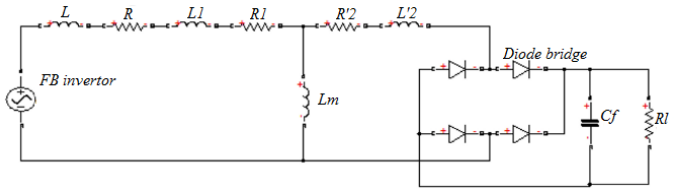


Figure 6. The equivalent circuit.

For influence analysis of the output filter capacity value on the primary winding current we use simulations with filters of different capacities. Output current and voltage plots of the inverter are shown in Fig.7 ($I_{i1}$ corresponds to capacity of 9900 μF of capacitors bank, $I_{i2}$ corresponds to capacity of 1100 μF).

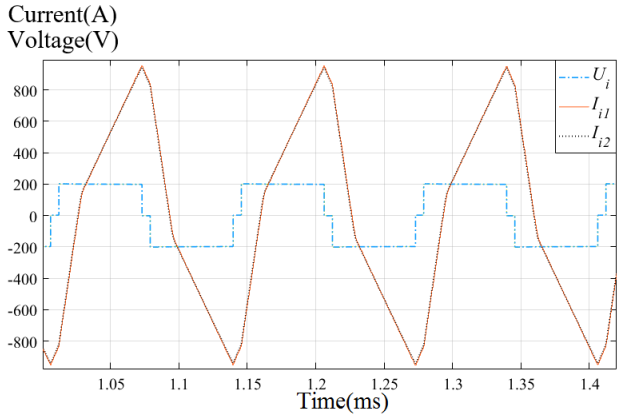


Figure 7. Output current and voltage plots of the inverter with different capacities.

Fig. 7 shows that current curves of primary winding with capacity of 9900 μF and with capacity of 1100 μF of capacitors bank are nearly do not differ from each other. So we can conclude that due to high value of capacity a simplified substitution connection can be considered for qualitative and approximate quantitative description of the

output inverter current as relation $(\omega C_f)^{-1} << R_l$ is correct. Fig. 8 shows simplified substitution connection where capacitor bank is substituted with ideal voltage source [17]. At short-circuiting of secondary winding through ideal voltage source relatively low current of transverse branch of the substitution transformer connection is not taken into account at calculations, so we can neglect magnetizing inductance. Then simplified substitution connection of transformer can be represented as *RL* circuit with parameters determined by parameters of transverse branch of the substitution connection shown in Fig. 1.

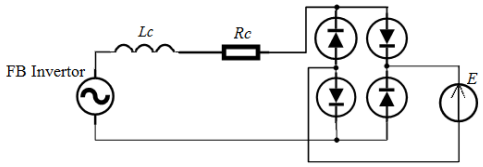


Figure 8. The simplified substitution connection.

Let us suppose that in fig.8 the inductance is $L_c = L + L_1 + L'_2$ and the resistance is $R_c = R + R_1 + R'_2$. Respect to the fact that *RL* time constant is greater than the carrier cycle, i.e. $L_c / R_c >> T_{PWM}$ ( $R_c \approx 0$ ), exponent transient responses could be changed by linear processes [18], so when a positive voltage pulse appears at the inverter output, the output current will grow linearly according to the law:

$$i(t) = U_{sv}(t - t_d) / L_c. \quad (1)$$

Due to Fig. 5 and Fig. 7 show steady-state processes, the beginning of positive current growth and the voltage jump are not synchronized and $t_d$ is time delay ( $U_{sv}$ is supply voltage).

Then the current will go up until the end of the voltage pulse, the maximum value of it will be equal to:

$$I_{\max} = U_{sv}(T_{PWM} K_{PWM} - t_d) / L_c. \quad (2)$$

At the end of the positive voltage pulse, the current will go down linearly according to the law, in which the reference time is beginning of zero-level of voltage:

$$i(t) = I_{\max}(1 - R_c t / L_c). \quad (3)$$

After the occurrence of a negative voltage pulse, the rate of current decay increases:

$$i(t) = I_{\max}(1 - R_c t / L_c) - U_{sv}(t - t_p) / L_c, \quad (4)$$

where $t_p$ is the time from reaching the maximum current to occurrence of the negative inverter output voltage.

It should be noted that in this section of the quasi-transient process a direction of an output inverter current does not coincide with the direction of the power source, i.e. the inverter supplies stored in the inductances energy to the power source. And the output inverter current lags behind the output inverter voltage.

The current will continue to go down until it becomes negative, the rectifier diodes will commutate, the polarity of the secondary winding voltage will change to the opposite, and the law of current variation will change to:

$$i(t) = -U_{sv}\, t / L_c, \quad (5)$$

where time *t* is measured from zero-crossing of current. The further process is identical to that described above, only current values are negative.

The qualitative description of the inverter output current curve requires knowledge of the value of the total inductance. Accurate calculation of the inductance value is impeded by its dependence on many plant parameters, which are adjusted during the debugging of the device. However, when some of parameters of the converter, the transformer and the capacitor bank are fixed, estimation technique the maximum permissible value of the total inductance $L_c$ could be really effective.

Estimation of the total inductance of the *RL* circuit can be obtained from (2):

$$L_c = U_{sv}(T_{PWM} K_{PWM} - t_d) / I_{\max}. \quad (6)$$

The maximum value of $L_c$ could be estimated from the fact that at pre-assigned values of $T_{PWM}$, minimum $K_{PWM}$ and maximum supply voltage $U_{sv}$ the transistor current should reach the possible maximum value, which is most often specified.

Fig. 9 ( $U_{sv}$ =320 V, $K_{PWM}$ =0.17) shows that for low value of $K_{PWM}$ time delay is approximately zero.

Then, according to the formula (6) and taking into account the fact that for a low value of $K_{PWM}$ $t_d = 0$:

$$L_c < U_{sv\_\max}(T_{PWM} K_{PWM}) / I_{\max}. \quad (7)$$

Let us write down method of selection the additional inductance value [19].

*Step 1*. The minimum value of the additional inductance is chosen by using the simulation: the maximum switched current value by the IGBT does not exceed a specified value with respect to given PWM carrier frequency, the maximum supply voltage and the minimum value of $K_{PWM}$.

*Step 2*. According to (7) find the necessary and sufficient value of the total inductance $L_c$ .


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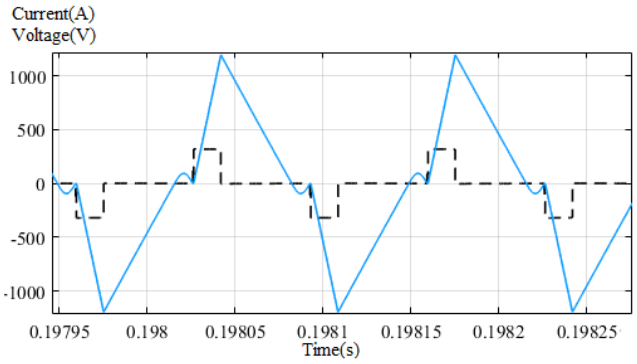


Figure 9. Output inverter current and voltage at $U_{SV}$=320 V, $K_{PWM}$=0.17.

*Step 3.* Calculate the transformer leakage inductance by using known techniques or from the (6) by using the experimental data without the additional inductance, estimate the value of the total inductance $L_C$ approximately.

*Step 4.* Having received the values of the transformer leakage inductance and $L_C$, estimate the value of the additional inductance.

*Step 5.* In practice, it should be taken into account that $K_{PWM}$ varies with voltage supply with regard to specified power roughly linearly. Therefore, the maximum total inductance should be set slightly less than the found one.

This technique is enough to specify parameters of the model. But because of the difficulty of measuring the transformer leakage inductance with sufficient accuracy, the maximum value of the additional inductance should be selected based on the experimental data.

To study the prototype, an additional inductance should not be exceeding value $0.6L_C$.

*Step 6.* If it is necessary, estimate the total resistance $R_c$ from the decreasing current section from expression (3) substituting a found value of $L_C$.

After estimation of $L_C$ and $R_c$ values it is possible to continue with analysis of thermal processes for the purpose of the transformer efficiency rise by variation of PWM carrier frequency for a prescribed range of supply voltage. Thermal processes calculation of power transistors should be carried out for average rectified current while energy balance of the system is calculated by average current of the inverter supply circuit.

As the third specific current section is absent for low values of $K_{PWM}$, then it is possible to estimate average output inverter current. From (1) for a known value of maximum current an expression for the first time section can be obtained in the form

$$t_1 = I_{\max} L_c / U_{sv}. \quad (8)$$

From (2) we have an expression for the second time section

$$t_2 = L_c / R_c. \quad (9)$$

Average output inverter current can be calculated if we divide sum of the two triangles' squares formed by currents of the first and the second sectors and the time axis by $T_{PWM}/2$,

$$I_{av} = I_{\max}(L_c / R_c + I_{\max} L_c / U_{sv}) / T_{PWM}. \quad (10)$$

It is more difficult to calculate average output inverter current for larger values of $K_{PWM}$, when we have three sectors of current. From (1)-(5) it is possible to obtain moments of time $t_d$ and $t_p$. But approximate estimation of average output inverter current is rather simple

$$I_{av} = I_{\max}/2. \quad (11)$$

The value of the average current is necessary for thermal calculation of power units.

It is important to estimate switching power losses of transistor modules. A known expression for transistors [17] can be used for this purpose

$$P_{SWC} = f_{sw}(E_{on} + E_{off}) \quad (12)$$

where $P_{SWC}$ is switching power losses in W, $f_{sw}$ is PWM carrier frequency in Hz, $E_{on}$, $E_{off}$ are energies released at switching on and off of the transistor module for corresponding switching currents.

It should be noted that transistors of the module switch on at zero current and switch off at the maximum current and zero collector voltage.

For PM800 transistors [15]: for switched current $I_s = 1250$ A from plots we find $E_{on}$ (for zero current) is about 5 mJ, $E_{off}$ is about 50 mJ. For PWM carrier frequency of 10 kHz switching losses of the module transistor are $P_{SWC} = 10000 \cdot 55/(1000) = 550$ W, for 7.25 kHz are 400 W. So we can conclude that optimal PWM frequency is 7.25 kHz. Increase of $K_{PWM}$ at increase of inverter supply voltage is achievable for fixed $I_{\max}$, $L_C$, $R_c$ only by increase of PWM carrier frequency which leads to increase of switching losses. So minimal operating frequency of the transformer and its characteristics which influence on $L_C$ are very important.

The minimum value of the additional inductance is chosen using the simulation: the maximum switched current value by the IGBT does not exceed a specified value with respect to the minimum PWM carrier frequency, the maximum supply voltage and the minimum value $K_{PWM}$. As average value of rated operating voltage (265 V) is 1.2 times less than

maximum supply voltage then required PWM carrier frequency for predetermined $I_{\max\_z} = 1250$ A is approximately 1.2 times more $\approx 8.7$ kHz.

For reduction of switching losses in prototype boost converter which is a part of frequency converter adaptive control is used, carrier frequency is changed in the interval 7.25…10 kHz depending on supply voltage 175...320 V: frequency increases when $K_{PWM}$ increases. Frequency converter is designed for power supply and control of an asynchronous motor of a compressor station drive by JSC Research Institute of Fine Mechanics (prototype is shown in Fig. 10). Boost converter is intended to perform in a small and confined space, so the main problems of its practical implementation are ensuring the load with the required power, reducing heat losses and high reliability. The prototype efficiency is 0.95. If we use equation (11) it is possible to make thermal calculation which proves appropriateness of the frequency variation.

Figure 10. Frequency converter (boost converter is on the left)

## IV. EXAMPLE

The transformer leakage inductance of the research prototype is known (it is conditioned by an elaboration of the transformer construction) and approximately equal to 1 μH. The minimum value of additional inductance is determined by simulation and equal to 2 μH. For specified characteristics $U_{sv\_\max} = 320$ V, $I_{\max\_z} = 1250$ A, the calculation should be carried out for maximum PWM frequency that is for $T_{PWM} = 10^{-4}$ s as $K_{PWM}$ varies with supply voltage with regard to specified power linearly, i.e. $K_{PWM}$ depends on relation $0.5 \cdot U_{sv\_min} / U_{sv\_max}$ and for (7) it could be defined as $K_{PWM} \approx 0.28$. Then $L_{C\max} = 6.94$ μH. With respect to step 5 the maximum value of additional inductance is $L_{\max} = 4.2$ μH.

The experimental data of 100kW industrial prototype with specified characteristics and the additional inductance is about $L = 3$ μH are provided below in Fig.11: (a) the full-bridge inverter output voltage $U_i$ (mirrored) and current $I_i$ (190V/div and 600A/div) $U_{sv} = 187$ V, $K_{PWM} = 0.35$, $f_{sw} = 10$ kHz; (b,c) the full-bridge inverter output voltage $U_i$ and current $I_i$ for a low value $K_{PWM}$ (190V/div and 1200 A/div) $U_{sv}$=320 V, $K_{PWM} = 0.18$, $f_{sw} = 7.25$ kHz. It is clear that simulation results in Fig.6 and Fig.9 and experimental results in Fig.11 are similar.

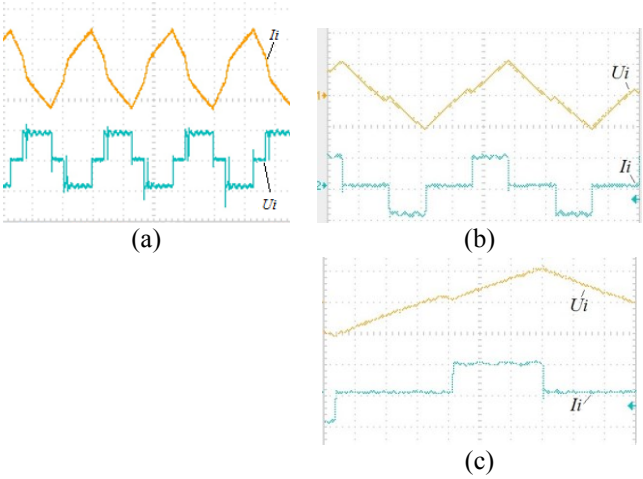


Figure 11. Experimental data.

Fig.11 illustrates that power switches work in the soft commutation mode, and it is possible to observe ZVS and ZCS for low value of $K_{PWM}$.

## REFERENCES

[1] Baei M., Narimani M., Moschopoulos G. A. “New ZVS-PWM Full Bridge Boost Converter,” Journal of Power Electronics. vol.14, 2014, pp.1-12.

[2] Koo G. B., Moon G. W., Youn M. J. “Analysis and design of phase shift full bridge converter with series-connected two transformers,” IEEE Trans. Power Electron., vol. 19, no. 2, 2004, pp. 411-419.

[3] Jang Y., Jovanovic M. M. “A new family of full-bridge ZVS converter,” IEEE Trans. Power Electron., vol. 19, no. 3, 2004, pp. 701-708.

[4] Jain P.K., Kang W., Soin H., Xi Y. “Analysis and design considerations of a load an line independent zero voltage switching full bridge DC/DC converter topology,” IEEE Trans. Power Electron., vol. 17, no. 5, 2002, pp. 649-657.

[5] Jang Y., Jovanovic M. M. “A new PWM ZVS full-bridge converter,” IEEE Trans. Power Electron.,” vol. 22, no. 3, 2007, pp. 987-994.

[6] Jeon S.J., Cho G. H. “A Zero-Voltage and Zero-Current Switching Full Bridge DC-DC Converter with Transformer Isolation,” IEEE Trans. Power Electron., vol. 16, no. 5, 2001, pp. 573-580.

[7] Sabate J.A, Vlatkovic Y., Ridel R.B., Lee F.C., Cho B. “Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter,” IEEE Applied Power Electronics Conference Proceedings 1990, pp.275-284.

[8] Delbin J.V., Rajaram M. “A new soft switched full bridge converter with voltage-doubler-type rectifier for high voltage applications,” International Journal of Computer and Electrical Engineering, vol.4, no. 2, 2012, pp.246-251.

[9] Zhu L. “A novel soft-commutating isolated boost full-bridge ZVS-PWM dc-dc converter for biderictional high power applications,” IEEE Trans. Power Electron., vol.21, no. 2, 2006, pp. 422-429.

[10] Chen B.Y, Lai Y.S. “Switching control technique of phase-shift-controlled full-bridge converte to improve efficiency under light-load


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and standby conditions without additional auxiliary components" IEEE Trans. Power Electron., vol.25, no. 4, 2010, pp. 1001-1012.

[11] Petrov R. "Optimum design of a high-power, high-frequency transformer," IEEE Trans. Power Electron., 1996, pp.33-42.

[12] Hurley W.G., Wilcox D.J. "Calculation of leakage inductance in transformer windings," IEEE Trans. Power Electron., vol.9, no. 1, 1994, pp. 121-126.

[13] Erickson R. W., Maksimovic D. "A multiple-winding magnetics model having directly measurable parameters," PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference , vol.2, 1998, pp. 1472-1478.

[14] Zhao L., Li H., Liu Y., Li Z. "High efficiency variable-frequency full-bridge converter with a load adaptive control method based on the loss model," Energies, 2015, pp. 2647-2673.

[15] Application manual. Intelligent power module PM800DV1B060 (http://www.mitsubishichips.com).

[16] Blache F., Pierre K., Cogitore B. "Stray capacitances of two winding transformers: equivalent circuit, measurements, calculation and lowering," Conference Record of the 1994 IEEE Industry Applications Society Annual Meeting, vol.2, 1994, pp. 1211-1217.

[17] Erickson R., Maksimovic D. Fundamentals of power electronics, Norwell, Mass: Kluwel Academic. 2001. 885 p.

[18] Charles K. A., Sadiku M. N. O. Fundamentals of electric circuits— 4th ed. McGraw-Hill. 2009, 1056 p.

[19] Alexandrova S., Baev A., Goncharenko M., Nikolaev N., Slita O. "Method of additional inductance selection for full-bridge boost converter," Proceedings of the International Scientific Conference on Physics and Control (Physcon 2017, Florence, Italy), (*to be published*).