Design of a new type of applied DC / DC Converter is a Current Sampling Circuit

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***Abstract*—This paper presents a power supply used in switching DC / DC converter new current sampling circuit, the main power drop by detecting switch series inductor current is sampled on to replace traditional detection sampling resistor voltage power on the bus on the drop method.Methods currently required less resistance, more efficient, low power consumption; and the drop of the inductor current changes in higher sensitivity, so better to improve the current sampling accuracy.**

Keywords-Current sampling; high precision; power switchIntroduction

The software ADINA is the product of the American company of ADINA, it is a large numeric calculational system based on the finite element method. It computes the engineering problems that various structure, fluid, the temperature field and several field coupling by solving various physical basic controlling equation. This paper recurs to the Pro/E and ADINA, making use of the parameterization design and numerical simulation, have researched siphonic bedpan's best structure of flow channel.

I. INTRODUCTION

In switching power DC/DC converter design, usually as a voltage feedback or current feedback control loop, current feedback loop is usually used as the inner ring, the basic stability of the whole system. Current loop principle is to detect the current through the switch, control switch is turned off, so as to maintain a stable output voltage. The sampling switch current in many ways, the power switch is usually a resistor in series with the sampling, the sampling resistor voltage drop is detected, so that the current sampling switch on. Focus of this design is to detect the power switch series inductance drop to sample the power tube current.

For DC/DC converters, mainly consists of power switch, freewheeling diodes, capacitors and feeling like point. Power switch in series with the inductor current has the same, so you can pass on the series inductor current sensing switch current reactive power, and to provide a basis for the power switch-off.

II. HARDWARE DESIGN

This article briefly describes the principles of traditional sampling circuit, then the voltage drop across the inductor details of current sampling methods to detect new series on the power switch.

A. Conventional current sampling circuit

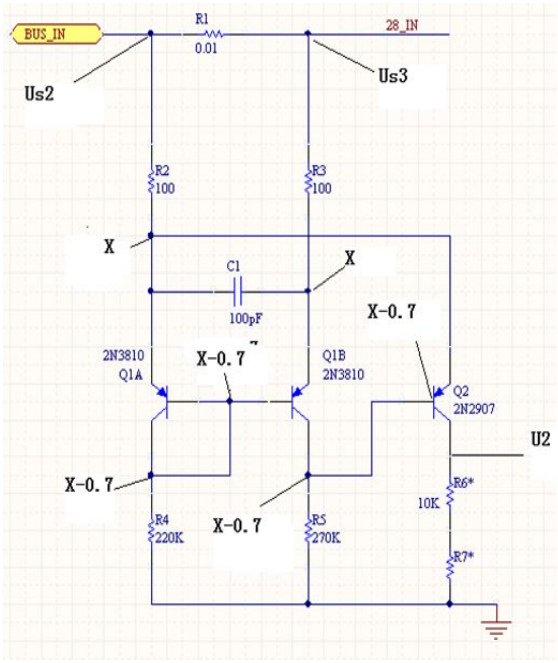

Figure 1. Sampling circuit simulation map

Conventional current sampling circuit diagram shown in Figure 1. The main function of the circuit through the sampling resistor R1 voltage variation on the bus and the external circuit through 2N3810 reflected.In the picture above is the sampling resistor R1, 2N3810 for the tube, R2 = R3, R4 = R5, R6 upper end of the current sampling output side, when the current increases power, current and voltage are larger on R1, R3 on current smaller, the R2 current larger, nearby tube 2N3810 current I1 = I2 = I3 = I4, then:

$$I_{R2} = I_{R3} + I_{Q2c}$$

So with the current big change on R2 also increases, the output voltage will be larger.

The relationship between the input and output voltage is:

$$U_2 = \frac{R_6}{R_2} \times U_1 \quad (U_1 = R_1 \times I_1) \tag{1}$$

As the power current increases, the sampling resistor on the bus power consumption will gradually become larger, in the case of high currents, this current sampling circuit will introduce large losses.

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B. The new inductor current sampling circuit

Traditional circuit has the disadvantages that loss increased because of the sampling resistor exists .In this paper circuit uses the advanced design ideas, effectively avoid the defect, taking into account the inductance DC / DC circuits essential device switch by measuring the voltage across the inductor in series, effectively avoid the introduction of alien resistance leads to increased losses.

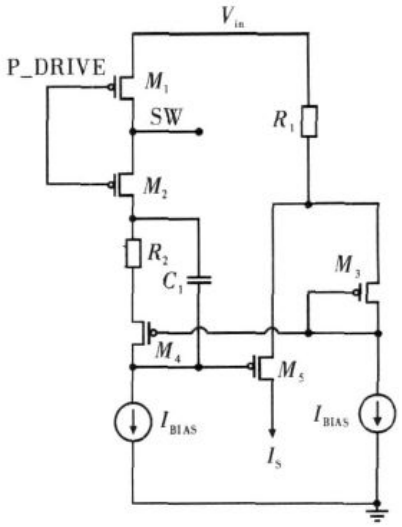

Figure 2. The new sampling circuit schematics

As shown in the schematic novel sampling circuit 2.In the figure 2, M3 ~ M5 and R1, C1 together constitute the sampling circuit, Vin is the power supply voltage, M1 main switch, M2 is the sampling switch, Ibias bias current signal, P_DRIVE drive signal for the switch, SW to access the series inductance of the access point switch, namely the detection point, this point voltage is the power switch on the voltage across the inductor in series; IS for the inductor current sampling output signal. Principle of novel sampling circuit utilizing a current rate of change is proportional to the voltage across the inductor to achieve both ends, namely

$$L\frac{dI_L}{dt}=V_L \tag{2}$$

①In the buck DC / DC converter circuit, SW detection points followed by the inductor get the output voltage Vo, the output voltage is very undecided, Vo approximately constant value. When opening MOSFET, inductor current increasing the voltage across the inductor can be expressed as:

$$V_L=V_{SW}-V_O \tag{3}$$

As can be seen from the above formula, VSM and the inductor voltage is linear, a VSM can reflect changes in inductor current.

② In boost or buck-boost DC/DC converter, SW detection point directly to ground through the inductor, so when the switch is turned on, the detected voltage SW point of inductor voltage, can react directly change the inductor current.

To sum up the above two cases, the switching power DC/DC converter, the series inductance of contact voltage Vsm reaction can change the amount of the inductor current, thus reflecting the current changes in the power switch.

According to the principle diagram, when the switch drive signal P_DRIVE high voltage, M1, M2 is turned off, the sampling circuit is in equilibrium, IS is zero.When P_DRIVE is low voltage, M1, M2 is turned on, the inductor current IL flowing through the main switch, the i-th switch on-resistance we set RES (ON) MPi, the main switch of the drop was:

$$V_{ON1}=V_{in}-V_{SM}=I_L\times RES(ON)_{MP1} \tag{4}$$

SW voltage detection points as follows:

$$V_{SM}=V_{in}-V_{ON1}=V_{in}-I_L\times RES(ON)_{MP1} \tag{5}$$

Sampling circuit M5 gate voltage is:

$$\begin{aligned}&V_{G5}=V_{SM}-I_{BLAS}*(RES\ (ON)_{MP1}\\&+RES\ (ON)_{MP4}+R_2)\end{aligned} \tag{6}$$

Source voltage of M5 is:

$$V_{S5}=V_{in}-(I_{BIAS}+I_S)\times R_1 \tag{7}$$

$$\begin{aligned}&V_{SG5}=V_{S5}-V_{G5}=I_{BLAS}*(RES\ (ON)_{MP2}\\&+(RES\ (ON)_{MP_4}+R_2-R_1)-I_s*R_1+I_L\\&*RES\ (ON)_{MP1}\end{aligned} \tag{8}$$

M5 tube according to the sampling circuit between the source-gate voltage current relationship:

$$I_S=0.5u_pC_0\left[\frac{W}{L}\right]_5(V_{SG5}-|V_{TH5}|)^2 \tag{9}$$

$$V_{SG5}=\sqrt{\frac{2I_S}{u_pC_0\left[\frac{W}{L}\right]_5}}+|V_{TH5}| \tag{10}$$

By Equation (8) and (10) can be drawn

$$\begin{aligned}&I_L\times RES(ON)_{MP1}=|V_{TH5}|+I_S\times R_1\sqrt{\frac{2I_S}{u_pC_0\left[\frac{W}{L}\right]_5}}\\&-I_{BIAS}\times(RES(ON)_{MP2}+RES(ON)_{MP4}+R_2-R_1)\end{aligned} \tag{11}$$

We can see from the equation, the greater when IL, IS the greater, IL smaller, IS smaller proportional relationship between the two, so that sampling current IS can reflect the change of the inductor current IL. Meanwhile switch series inductance voltage compared to the changing circumstances of the inductor current to be sensitive to the sampling resistor, so the sampling precision is higher.

III. THE NEW INDUCTOR CURRENT SAMPLING CIRCUIT SIMULATION

In order to verify the accurateness of the new sampling circuit sampling accuracy,enter the sawtooth voltage into power switch, and then look at the output voltage with the original sawtooth voltage case and precision tracking situation.The presence of voltage fluctuations 0.5mv in the sawtooth voltage waveform ,reference voltage is 100mV,up and down the 0.25mv,as shown in figure 3:

In case there is a slight input voltage changes, the output voltage will appear a substantial voltage amplification,The simulation results of the new sampling circuit output voltage is as follows:

The theoretical value of output voltage should 5V float,however, given the loss of the main switch and the sampling switch itself, not theoretically zero,therefore, the average output voltage will drop.The two figures into the same graph as shown in Figure 5.

As can be seen from the chart,the circuit fully realized amplified voltage signal,at the same time tracking the input signal effectively ,realized the synchronization with the input signal under the premise of voltage amplification.

IV. CONCLUSION

This paper describes the current feedback loop sampling current DC / DC switching power converter generating circuit,and commonly used sampling methods and new sampling methods are analyzed and compared.The text of the current sampling circuit design required less resistance, thereby reducing the power consumption and improve the efficiency;Since the voltage drop across the inductor and higher sensitivity change, thereby improving the accuracy of sampling.Thus, the performance of the new sampling circuit has been greatly improved over traditional methods, being available to a reference for the sampling circuit .

REFERENCES

[1] Behzad Razav.i Design ofAnalog CMOS Integrated Cir-cuits [M]. Xipan: Publishing House of Xipan Jiaotong University, 2003.

[2] Phillip E, Allen Douglas, Holberg R. CMOS Analog CircuitDesign [M]. Second Edition. Beijing: Publish-ingHouse ofElectronics Industry, 2002.

[3] Paul R Gray, Paul J Hurst, Stephen H Lewis, et a.l Analysis and Design ofAnalog Integrated Circuits [M].4E. Newyork: JohnW iley& Sons, 2000.

[4] Midya P, Greuel M, Krein P T. Sensorless current mode control-an observer-based technique for DC-DC converters[J]. IEEE Transations on Power Electron-ics, 2001, 16(4):522-526.

[5] Forghani-zadeh H P, Rincon-Mora G A. Current-sensing techniques for DC-DC converters[C]. Mid-west Symposium on Circuits and Systems, 2002:577-580.

[6] Dallago E, Passoni M, Sassone G. Lossless current sensing in low-voltage high-current DC/DC modular supplies[J]. IEEE Transactions on Industrial Elec-tronics, 2000,47(6):1249-1252.

[7] Wang shui-ping,Wu mang,Peng xue-yu.Switching power supply and developments[J]. Electronic Science and Technology,1996(4): 3-10.

[8] Tian jin-ming,Wang song-lin,Lai xin-quan,and so on.Low Power Dissipation Design of AC/DC Switched Mode Power Controller[J].Electronic Science and Technology,2006(6):11-14.

[9] Franco S. DesignwithOperationalAmplifiers andAnalog Integrated Circuits [M]. Second Edition. Newyork:McGrawHil,l 1998.

[10] Cheung F L, Mok P K T. A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique [J]. IEEE Journal of Solid-state Circuit, 2004,39(1):3-14.

[11] Kimball J W, Mossoba J T, Krein P T. A stabilizing, high-performance controller for input series-output parallel converters[J]. IEEE Transactions on Power Electronics, 2008,23(3):522-526.

[12] Choksi O, Carley L R. Analysis of switched-capacitor common-mode feedback circuit [J]. IEEE Transac-tions on Circuits and Systems II: Analog and Digital Signal Processing, 2003,50(12):906-917.

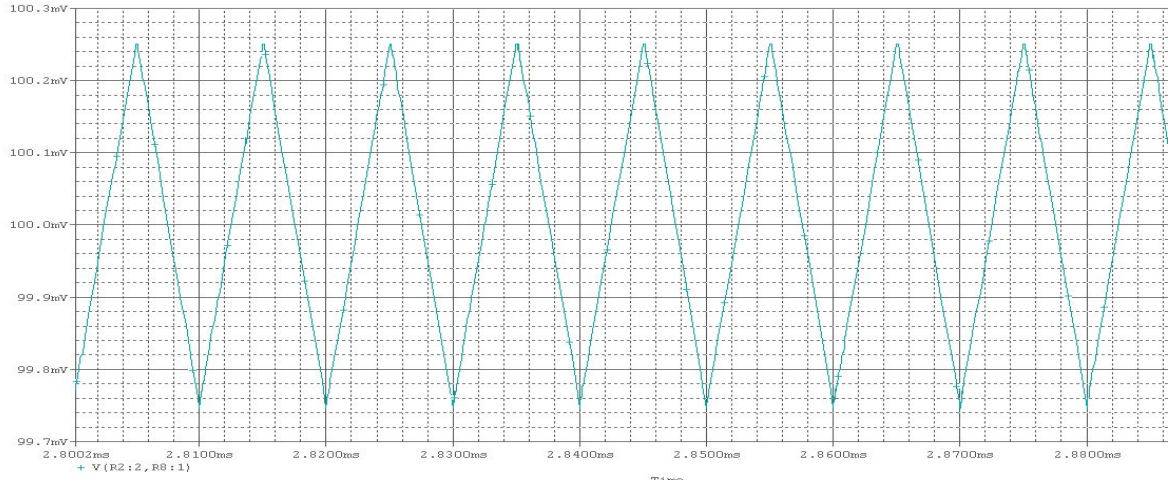

Figure 3. Sampling circuit input voltage waveform

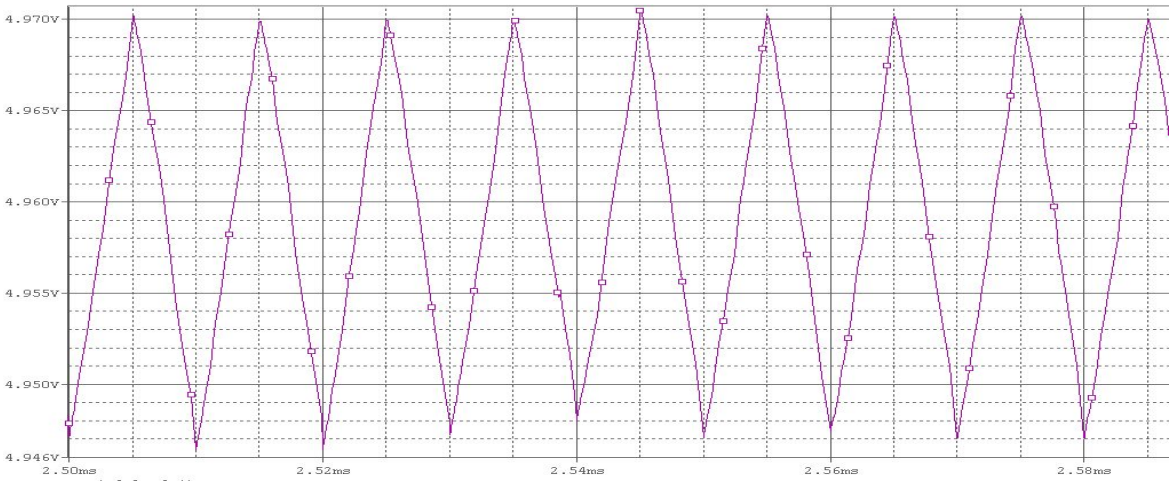

Figure 4. Sampling circuit output voltage waveform

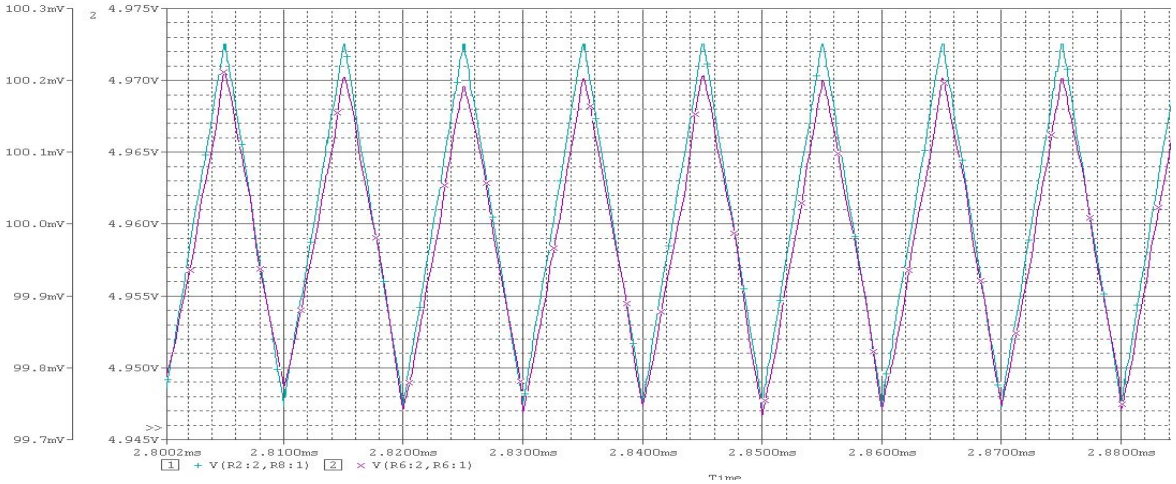

Figure 5. Sampling circuit input and output voltage comparators