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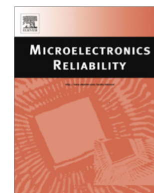

Variability and reliability analysis of CNFET technology: Impact of manufacturing imperfections

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ABSTRACT

Carbon nanotube field-effect transistors (CNFETs) are promising candidates to substitute silicon transistors. Boasting extraordinary electronic properties, CNFETs exhibit characteristics rivaling those of state-of-the-art Si-based metal–oxide–semiconductor field-effect transistors (MOSFETs). However, as any technology that is in development, CNFET fabrication process still have some imperfections that results in carbon nanotube variations, which can have a severe impact on the devices' performance and jeopardize their reliability (in this work the term reliability means time-zero failure due to manufacturing variations). This paper presents a study of the effects on transistors of the main CNFET manufacturing imperfections, including the presence of metallic carbon nanotubes (m-CNTs), imperfect m-CNT removal processes, chirality drift, CNT doping variations in the source/drain extension regions, and density fluctuations due to non-uniform inter-CNT spacing.

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1. Introduction

The aggressive scaling down of the physical dimensions of metal–oxide–semiconductor field-effect transistors (MOSFETs) has required the introduction of a wide variety of innovative factors to ensure that they are still properly manufactured. However, with each new generation of MOSFETs, and the resulting shrinking of the devices' dimensions to an atomistic scale, the manufacturing challenges have become more difficult, and statistical variability has emerged as a key issue [1]. According to the International Technology Roadmap for Semiconductors (ITRS) [2], intensive research is needed to continue this process and to develop new devices and methods to steer the technology improvements in other directions.

In recent years, carbon nanotubes (CNTs) have been attracting considerable attention in the field of nanotechnology. They are considered to be a promising substitute for silicon because of their small size, unusual geometry (1D structure), and extraordinary electronic properties, including excellent carrier mobility and quasi-ballistic transport [3,4].

Carbon nanotube field-effect transistors (CNFETs) could be potential substitutes for MOSFETs [5,6]. "Ideal" CNFETs (meaning all CNTs in the transistor are semiconducting, have the same diameter, and are aligned and well-positioned) are predicted to be 5$\times$ faster than silicon CMOS, while consuming the same power [7]. However, CNFETs are also affected by manufacturing variability [8,9], and several significant challenges must be overcome before these benefits can be achieved. Certain CNFET manufacturing imperfections, such as CNT diameter and doping variations, mispositioned and misaligned CNTs, the presence of metallic CNTs (m-CNTs), and CNT density variations, can affect CNFET performance and reliability and must be addressed. Note that in this work the term reliability refers to failures in CNFETs because of CNT variations that results from manufacturing imperfections (time-zero failures).

In [10] how CNFET manufacturing variations (including CNT diameter and doping variations, the presence of m-CNTs, and the imperfections of m-CNT removal processes) affect the radio frequency performance of CNFET devices and circuits was analyzed. The effects of CNT count variations (CNT density variations + perfect removal of m-CNTs) on CNFET devices and digital circuits were studied in our previous publication [11] and in [12], respectively. In this paper, we will analyze the impact of these and all the other CNFET manufacturing challenges mentioned above on multi-channel CNFET variability and reliability in different m-CNT removal scenarios. To this end, the rest of the paper is organized as follows: Section 2 reviews the main imperfections inherent in the CNFET manufacturing process as well as the main challenges for achieving high-performance CNFETs, Section 3 describes the CNFET model and variability analysis methodology using Monte Carlo

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simulations, Section 4 discusses a CNFET variability study, Section 5 presents an analytical CNFET failure model, and Section 6 presents the conclusions.

2. Manufacturing imperfections in CNFETs and challenges

As any technology that is in development, CNFET manufacturing process still have some imperfections, including:

- *The alignment and positioning of the CNTs during the CNT growth process*: CNTs grown on quartz substrates can yield nearly perfectly linear (>99.9%) aligned arrays of CNTs [13], but there remains a non-negligible fraction of mispositioned CNTs that can interfere with the logic functionality. Nevertheless, CNFET circuits immune to such mispositioned CNTs have been developed [14].
- *CNT diameter variations*: Chirality is responsible for the CNT diameter. Since the band-gap of CNTs is strongly dependent on diameter, accurate control of the diameter is essential to the performance of CNFETs. Diameter variations cause fluctuations in the CNFET's threshold voltage and drive current. Typical CNT growth techniques produce CNTs with diameters ranging from 0.5 to 3 nm, but the standard deviation of the CNT diameter can often be controlled within 10% of the mean diameter [13].
- *CNT doping variations*: These variations refers to the variations of the doping concentration in the source/drain extension regions of a CNFET. It is worth noting that CNFETs, specially n-type CNFETs, need to be doped to give the transistor its polarity.
- *CNT density variations* [15,11]: These variations are due to the non-uniform spacing between CNTs (non-uniform pitch) during CNT growth, resulting in variations in the number of CNTs in the transistor (CNT count variations). Not only do they cause large variations in CNFET performance, but they also lead to a significant probability of complete failure in cases where there are no CNTs present in the CNFET (opens).
- *The presence of metallic CNTs among semiconducting CNTs (s-CNTs)*: Metallic CNTs should not be used to make CNFETs because their high conductivity makes it impossible to control the current with the gate, thereby causing source-to-drain shorts in the CNFET. In a typical CNT synthesis process, 1/3 of CNTs are metallic and 2/3 are semiconducting. In order to reduce the proportion of m-CNTs, different processing options can be used. One option is to grow predominantly s-CNTs. Enhanced CNT growth methods can be used to achieve a percentage of s-CNTs between 90% and 96% [18,19]. Another alternative is to separate the m-CNTs from the s-CNTs after the CNT growth to obtain mostly s-CNTs. In this regard, a considerable reduction in the percentage of m-CNTs (to 1–5% m-CNTs) has also been achieved with CNT self-sorting techniques [20]. However, this improvement in the percentage of m-CNTs is not enough for very-large-scale integration (VLSI) digital circuits. For high-performance logic applications, which would require billions of transistors, the impurity concentration of m-CNTs would need to be less than 0.0001%. A third processing option is thus to remove the m-CNTs after the CNT growth. Existing techniques for m-CNT removal include single-device electrical breakdown (SDB) [21], gas-phase and chemical-reaction-based removal techniques [22], and VLSI-compatible metallic-CNT removal (VMR) [23]. SDB removes ~100% of m-CNTs, but it is not VLSI-compatible. Gas-phase chemical-reaction-based removal techniques are highly compatible with VLSI semiconductor processing, but m-CNT removal depends on CNT diameters, and a narrow CNT diameter distribution is required. Finally, VMR is VLSI-compatible but can impose area penalties. Furthermore, non of all these m-CNT removal techniques is perfect; some m-CNTs still survive after m-CNT removal, while a non-negligible fraction (typically, 10–40%) of the s-CNTs can accidentally be eliminated during the process. As a result, the number of CNTs in the transistor decreases, thereby increasing the likelihood of failure (opens). A novel and promising approach for m-CNT removal called thermocapillary-resist was recently presented in [24]. This technique has been used to achieve the highly selective of m-CNTs from the full length of an aligned array of CNTs on a chip without damaging the s-CNTs. However, it must be improved before it can be used with very high CNT densities.

It should be noted that all of the above CNT imperfections are typical of the CVD method. Another approach is to use solution-processed CNTs [25]. With this method, the CNTs are first suspended in solution, and then separated, assembled, and deposited onto substrates for device fabrication. This process offers unique processing advantages over the CVD method, including the capabilities of separating nanotubes by electronic type (with s-CNT purity of over 99%) and depositing them onto various substrates in the form of ultradensely aligned arrays at low temperature. However, long-channel CNFETs that use solution-processed CNTs generally show inferior device performance due to the presence of a higher number of structural defects.

In addition, the realization of high-performance CNFETs requires advances in the following areas:

- *Increased CNT density*: The most used method for growing CNTs is chemical vapor deposition (CVD). CNT arrays are grown on a quartz wafer. They are then transferred onto a target substrate (e.g., a silicon wafer) for circuit fabrication. The average CNT density obtained today with this technique is in the range of 1–10 CNTs/μm. Multiple-growth or multiple-transfer techniques [16,17] can increase the CNT density up to 45–55 CNTs/μm. However, that is still significantly lower than the CNT density required for logic circuits, i.e., 250 CNTs/μm. This notwithstanding, higher CNT densities (more than 500 CNTs/μm) can be obtained using other methods such as the Langmuir–Schaefer technique [26].
- *Controlling the CNT doping process*: Digital circuits require n-type and p-type CNFETs. High-performance p-type CNFETs have been developed using high-work-function metal contacts, but the development of n-type CNFETs that are stable in ambient air remains a challenge. However, recent studies have demonstrated functional n-type CNFETs using low-work-function metal contacts [27] and ALD-based electrostatic doping [28].
- *Achieving low metal-to-CNT contact resistance*: The lowest theoretically achievable contact resistance is 6.5 kΩ, the quantum limit. However, this resistance is hard to achieve because of the poor wetting properties of metal to CNTs and the presence of Schottky barriers (SBs) between the CNT and the metal due to band misalignment. Solutions include the use of graphitic carbon interfacial layers to increase the contact area between the metal and the CNT [29] and the selection of a proper work-function metal contact [30] to reduce the SB.

For CNFET digital logic applications, multi-channel CNFETs are required. In these devices, the main sources of variability and failure are the presence of m-CNTs and CNT count variations due to density fluctuations and m-CNTs that are subsequently removed. They are followed by variations in diameter, doping and alignment. The latter factors have a minor impact on circuit performance because of statistical averaging. Thus, many papers have been published recently related to the functional yield of CNFET circuits in

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the presence of metallic CNTs and CNT density and count variations [15–29,31–33].

3. Impact of CNFET manufacturing imperfections on transistor performance

In this section, we present a methodology of analysis based on a MATLAB script to study the effect that the main CNFET manufacturing imperfections have on CNFET characteristics and transistor parameters when different m-CNT removal techniques are considered.

3.1. Nominal CNFET device

In our study we use the CNFET compact model developed by Stanford University [34–36]. It is a MOSFET-like CNFET that uses a top-gate structure. It consists of N perfectly aligned and positioned s-CNTs whose section under the gate is intrinsic and whose source/drain extension regions are n- or p-doped (p-type or n-type transistors). We consider as nominal a CNFET that is composed by 7 CNTs. The chirality of the CNTs is (19,0), giving them a diameter of $\sim$1.5 nm. The inter-CNT spacing, or pitch, is 4 nm which translates to a density of 250 CNTs/μm (taking into account the inter-CNT electrostatic charge screening effect [37]). The length of the gate, source and drain (L_{ch}, L_{ss}, L_{dd}) is 16 nm. The width of the gate is 28 nm (W_{gate}). We considered ohmic metal contacts (as with high CNT doping of $\sim$0.8% and similar metal and CNT work functions, $\Phi_C = \Phi_M$ = 4.5 eV, the SB resistance could be suppressed to a low value of <1 kΩ).

An n-type 7-tube CNFET was simulated using the Stanford CNFET model. The key transistor parameters were: $I_{ON} = 57.89$ μA, $I_{ON}/I_{OFF} = 1 \times 10^6$ and $V_{TH} = 0.29$ V. The ON current (I_{ON}) and ON–OFF current ratio (I_{ON}/I_{OFF}) were extracted from I–V characteristics. I_{ON} is the current when $V_{DS} = V_{GS}$ = 0.9 V, and I_{OFF} is the current when V_{DS} = 0.9 V and V_{GS} = 0 V. The threshold voltage (V_{TH}) was obtained using the well-known expression [36]

$$V_{TH} = \frac{E_g}{2q} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \quad (1)$$

where $a = 2.49$ Å is the carbon-to-carbon-atom distance, $V_\pi = 3.033$ eV is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter ($D_{CNT} = (\sqrt{3}/a_0)\sqrt{n^2 + m^2 + nm}$).

Note that this CNFET model does not include variability aspects. In other words, it can only be used to simulate transistors with one or more s-CNTs with the same diameter, doping and inter-CNT spacing.

3.2. Procedure for analyzing CNFET manufacturing variability

A methodology of analysis based on a MATLAB script was used to analyze the variability of transistor characteristics and parameters due to the following CNFET manufacturing imperfections: (i) variation in CNT diameter; (ii) variation in CNT density due to non-uniform spacing between parallel CNTs in multi-channel CNFETs; (iii) the presence of m-CNTs in the transistor; and (iv) variations in CNT doping. The study did not consider mispositioned CNTs because CNFET circuits have been developed that are immune to them and we assumed ohmic CNT-metal contacts.

The CNFET variability methodology is suitable for different scenarios: (i) no m-CNT removal; (ii) non-ideal m-CNT removal processes in which some s-CNTs are removed and all or nearly all m-CNTs are removed; and (iii) ideal m-CNT removal techniques that remove all m-CNTs but leave all s-CNTs intact. Fig. 1 and Table 1 show the MATLAB script structure and the distributions of the variable parameters, respectively.

In the CNFET sample extraction stage, in step 1 the number of CNTs (N) in the transistor is obtained for given gate width (W_{gate}) and pitch distribution (P). The proportion of m-CNTs and s-CNTs is then established using a given probability that a CNT is metallic (p_m) and for given diameter (D) and doping (Dop) distributions (step 2). In step 3, the final number of CNTs is determined (n) based

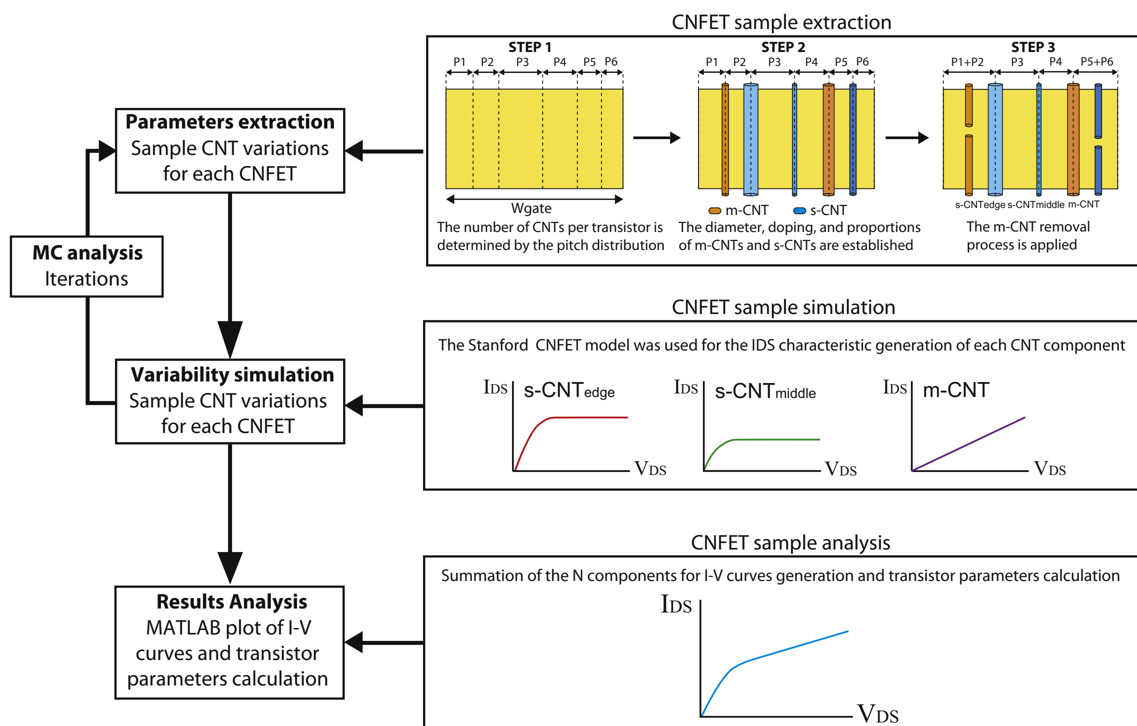

Fig. 1. Monte Carlo process simulation using our MATLAB script.

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Table 1
Distributions used in Fig. 1 and Sections 4 and 5.

	Distribution	Ref.
CNT diameter (D)	Normal: $\mu_{dia} = 1.5$ nm, $\sigma_{dia} = 0.16$ nm	[13]
Pitch (P)	Chi^2: $\mu_{pitch} = 4$ nm, $\sigma_{pitch} = 0.16$ nm	[15]
S/D doping level (Dop)	Normal: $\mu_{dop} = 1\%$, $\sigma_{dop} = 0.1\%$	[7]
m-CNT probability (p_m)	Uniform: 0–33%	[7]
m-CNT removal prob. (p_{mR})	Uniform: 99.99–100%	[22,23]
s-CNT prob. (p_{sR})	Uniform: 10–40%	[22,23]

on the probability that a CNT is removed given it is an m-CNT (p_{mR}) or s-CNT (p_{sR}). The pitch of the remaining CNTs is then recalculated. Hence, the result of the CNFET sample extraction stage is a sample of n-tube CNFET, with a mixture of m-CNTs and s-CNTs with different diameters, different S/D doping levels, and different inter-CNT spacing.

In the CNFET sample simulation and CNFET sample analysis phases, the *I–V* characteristics of the n-tube CNFET sample were obtained. This was done through the summation of the *n* I_{DS} current components (each CNT forming the CNFET) obtained with the Stanford CNFET model, taking into account the charge screening effects and the tube's position in the transistor (edge or middle) (Fig. 1). Note that for CNFET with multiple parallel CNTs and an inter-CNT pitch smaller than 20 nm, the CNT-to-CNT screening affects both the gate-to-channel electrostatic capacitance and the drive current. The current delivered by each m-CNT was calculated based on equations presented in [34,35].

3.3. Simulation results

Using the procedure described in the previous section, we performed 10,000 Monte Carlo (MC) simulations for a multi-channel CNFET with an average of $N = 7$ CNTs ($W_{gate} = 28$ nm, $\mu_{pitch} = 4$ nm) for the following three cases of m-CNT removal:

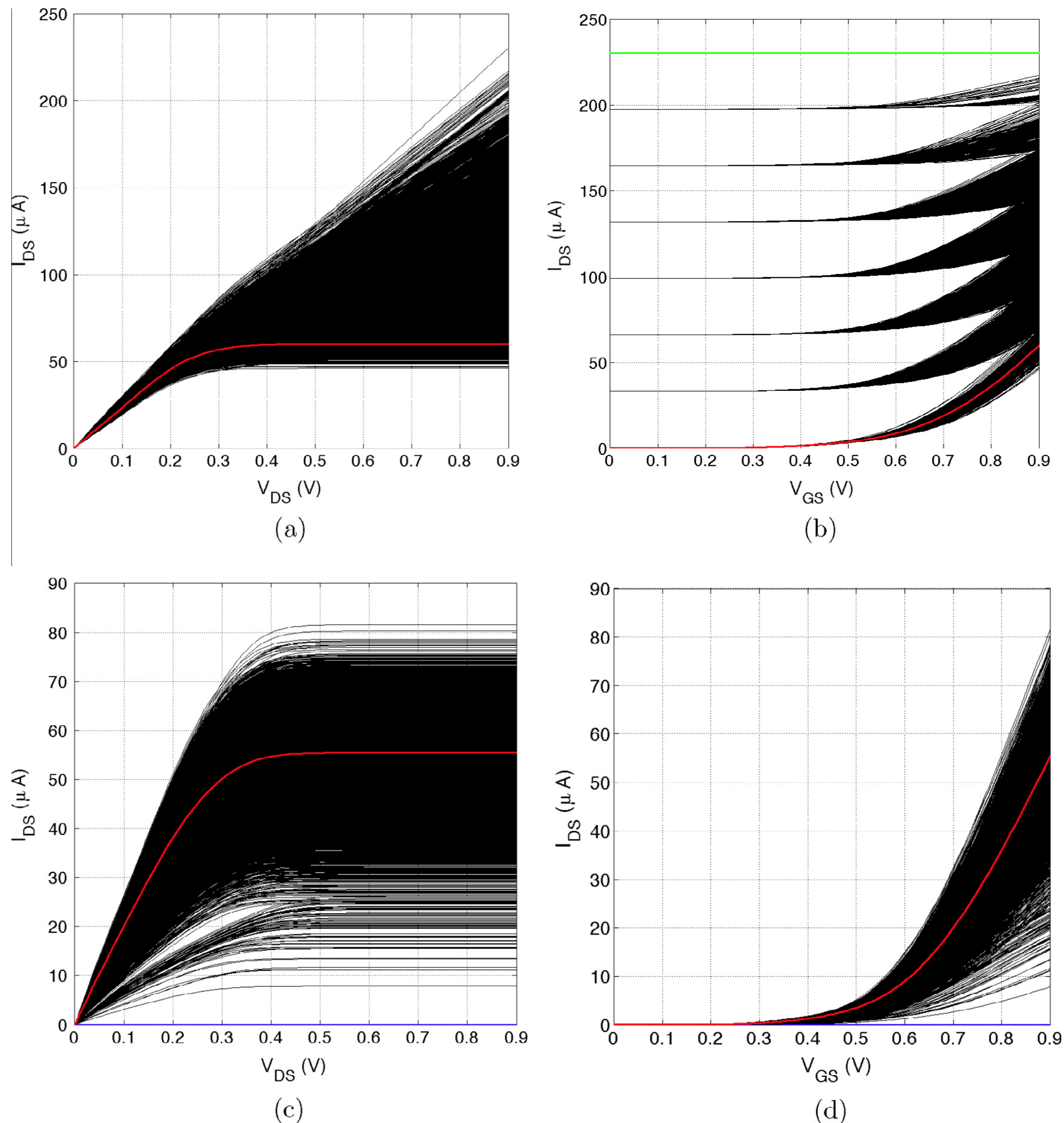

Fig. 2. I-V CNFET characteristics for an n-type CNFET and $p_m = 33\%$ when no m-CNT removal technique is used (a and b) and when ideal m-CNT removal technique is considered (c and d). The curves for the 10,000 simulated devices (black curves) are shown, along with the average of the functional CNFETs (red curve). The green line in (b) is full shorts, whereas the blue line in (d) is opens. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

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1. No m-CNT removal ($p_{mR} = p_{sR} = 0\%$).
2. Non-ideal m-CNT removal technique: all m-CNTs and some s-CNTs are removed ($p_{mR} = 100\%$ and p_{sR} = 10–40%) or just a small portion of the m-CNTs survives ($p_{mR} = 99.99\%$ and p_{sR} = 10–40%).
3. Ideal m-CNT removal technique ($p_{mR} = 100\%$ and $p_{sR} = 0\%$).

Moreover, for each m-CNT removal scenario, we considered four different m-CNT probabilities: $p_m = 33\%$ (typical CNT growth methods) and $p_m = 10\%, p_m = 5\%$, and $p_m = 1\%$ (enhanced CNT synthesis methods and self-sorting techniques).

The current characteristics (I_{DS}–V_{DS} and I_{DS}–V_{GS}) for m-CNT elimination scenarios (1) and (3) and for the worst case of m-CNT probability ($p_m = 33\%$) are shown in Fig. 2. The *I–V* curves for m-CNT removal case (2) are not shown because they are similar to those for (1). The results of this simulation will be analyzed in the following sections.

Probit plots of I_{ON} and I_{OFF} when m-CNTs are not removed and when an ideal m-CNT removal process is considered are depicted in Fig. 3. These plots complement the *I–V* current characteristics showed in the previous Figure and the data shown in Table 2.

4. Variability analysis

Based on the I_{DS}–V_{GS} current distributions obtained with the CNFET manufacturing variability methodology presented in Section 3.3, and taking into account only the functional transistors when an ideal m-CNT removal technique is applied (i.e., ignoring opens), we calculated the mean (μ) and standard deviation (σ) for several key transistor parameters: $I_{ON}, I_{ON}/I_{OFF}$ and V_{TH} (Table 2).

With regard to the behavior of μ and σ vs. p_m, it can be seen that in the case of I_{ON}, the mean increases slightly as p_m decreases, whereas the STD decreases. For I_{ON}/I_{OFF}, both the mean and the STD decrease slightly as p_m decreases. Finally, V_{TH} remains almost constant for all four p_m as in this study we considered it to be affected only by diameter variations. However, in terms of variability, the I_{ON} and I_{ON}/I_{OFF} parameters are highly affected by CNT count variations, yielding variability values ($3\sigma/\mu$) between 46.98% and 185.67% ($p_m = 33\%$) and 24.89% and 96.81% ($p_m = 1\%$), respectively.

Threshold voltage presented a more moderate fluctuation of about 12%.

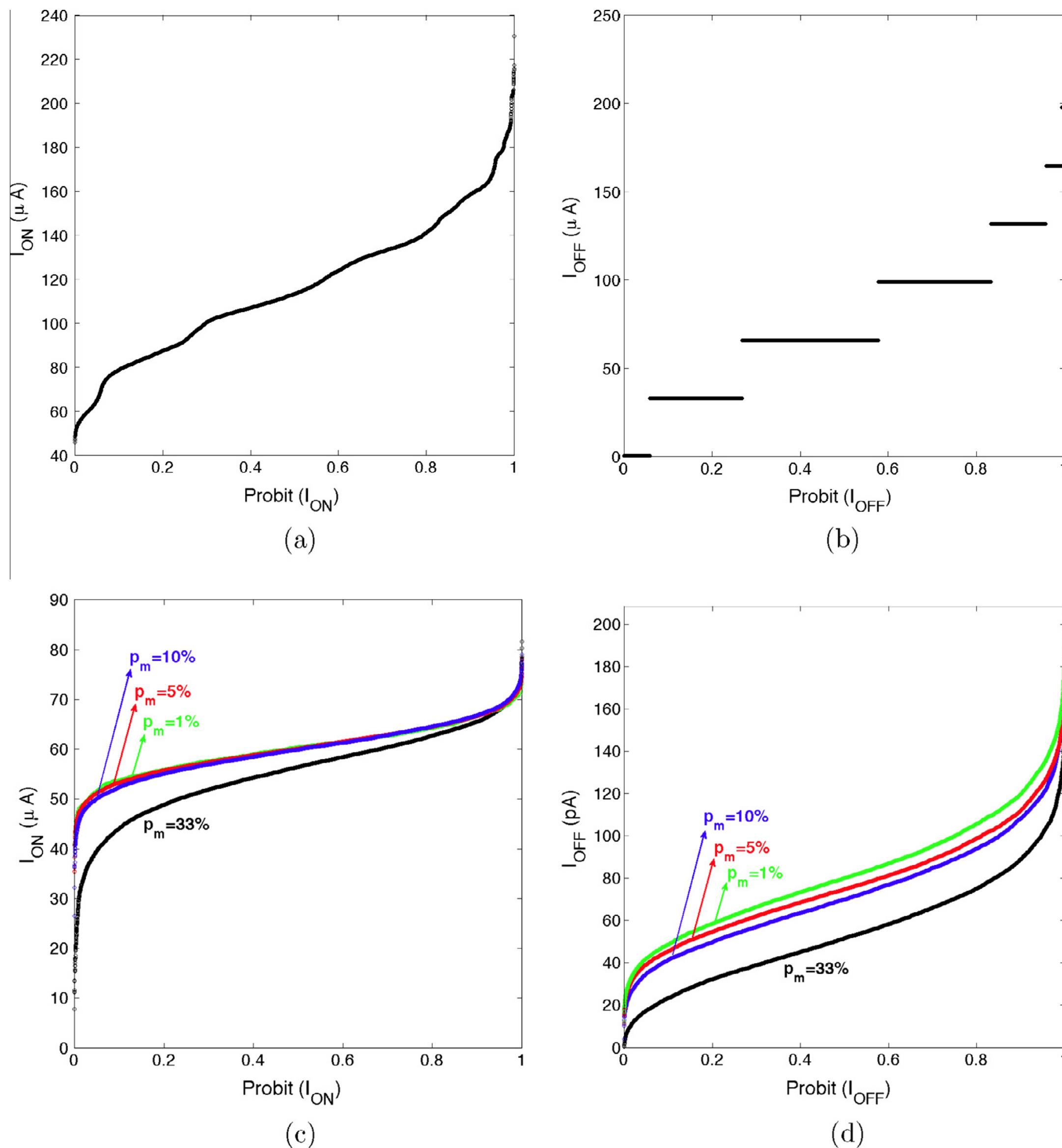

Fig. 3. Probit plots of I_{ON} and I_{OFF} when no m-CNT removal technique is used and for $p_m = 33\%$ (a and b) and when ideal m-CNT removal technique is considered and for four different p_ms (c and d).

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Table 2
Mean and STD when ideal m-CNT removal technique is applied (only functional transistors).

	$p_m = 33\%$		$p_m = 10\%$		$p_m = 5\%$		$p_m = 1\%$	
	μ	σ	μ	σ	μ	σ	μ	σ
I_{ON} (μA)	55.47	8.78	59.75	5.69	60.06	5.24	60.14	4.99
I_{ON}/I_{OFF} ($\times 10^5$)	12.7	7.86	9.25	3.37	8.60	2.81	8.15	2.63
V_{TH} (V)	0.26	0.02	0.26	0.02	0.26	0.01	0.25	0.01

It is worth noting that in the case considered (ideal m-CNT removal method, $p_{mR} = 100\%$), it is possible to achieve a very high I_{ON}/I_{OFF} in the order of 10^5–10^6. However, the presence of m-CNTs severely degrades it. As shown in [31], the I_{ON}/I_{OFF} ratio of a CNFET composed of a mixture of s-CNTs and m-CNTs can be calculated as:

$$\frac{I_{ON}}{I_{OFF}} = \frac{N_s I_{s,on} + N_m I_m}{N_s I_{s,off} + N_m I_m} \quad (2)$$

where N_s and N_m are the number of s-CNTs and m-CNTs, respectively; $I_{s,on}$ and $I_{s,off}$ are the ON and OFF currents of an s-CNT as defined in Section 3.1 above; and I_m is the current delivered by an m-CNT when $V_{DS} = 0.9$ V, and it is the same for both the ON and OFF states. When the CNFET circuit level is considered (for multiple transistors), the most adequate parameter is the ratio of the mean values of I_{ON} and I_{OFF}:

$$\frac{\mu(I_{ON})}{\mu(I_{OFF})} = \frac{\mu(N_s)\mu(I_{s,on}) + \mu(N_m)\mu(I_m)}{\mu(N_s)\mu(I_{s,off}) + \mu(N_m)\mu(I_m)} \quad (3)$$

where

$$\frac{\mu(N_s)}{\mu(N_m)} = \frac{p_s(1 - p_{sR})}{p_m(1 - p_{mR})} \quad (4)$$

when an m-CNT removal process is applied.

Using these equations and the mean of the ON and OFF currents obtained through the 10,000 MC simulations, Fig. 4 illustrates how the presence of m-CNTs in the transistors affects the average I_{ON}/I_{OFF} ratio for the four p_m probabilities assumed and for different p_{sR}. It should be observed that the average ratio improves as p_m and p_{sR} decrease and p_{mR} increases as expected. It should likewise be noted that this ratio remains almost constant once p_{mR} approaches 100%. Moreover, it is in the range of 10^5–10^6 (inset in Fig. 4) and fluctuates slightly as the p_m changes, as seen in Table 2.

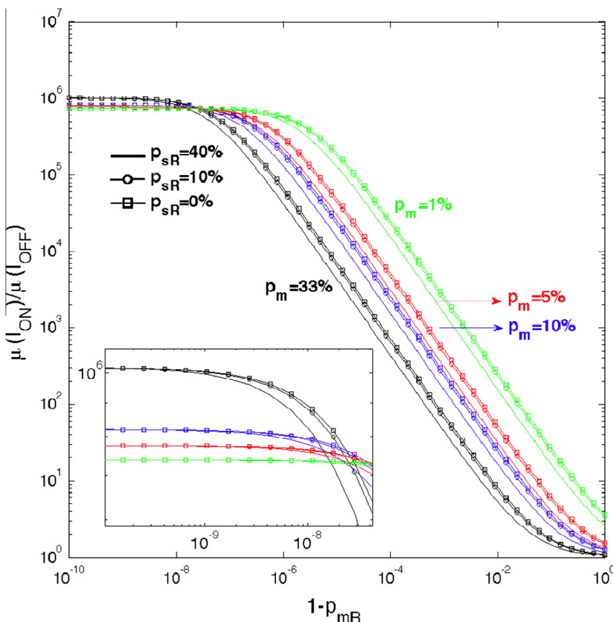

Fig. 4. Average I_{ON}/I_{OFF} ratio vs. probability of m-CNT survival. (Inset) Zoom when $1 - p_{mR}$ is between 10^{-7} and 10^{-10}.

5. Statistical reliability analysis

The main causes of failure in CNFETs are the presence of m-CNTs in the transistor and CNT count variations due to density fluctuations and the application of m-CNT removal processes. An open occurs when there is no CNT bridging the source and drain contacts; a short is caused by the presence of one or more m-CNTs in the transistor.

Many previous publications have presented analytical models to evaluate the impact of CNT density and count variations and of m-CNTs on CNFET devices and circuits. In [32], a compact model for the probability of failure in CNFETs is presented that includes m-CNTs and density variations based on a binomial probability distribution. In [15], a probabilistic framework for modeling the CNT count distribution in a CNFET of a given width is developed and used to estimate the CNT count yield of a CNFET when an ideal m-CNT removal process is applied. That model thus takes only open defects into account.

As an extension of these two previous analytical models, a CNFET failure model is derived and presented in this section. CNFET failure model proposed in [32] considers both open and short defects that are due to CNT density variations ("void CNFET") and the presence of m-CNTs, respectively. That is, m-CNTs are not removed ($p_{mR} = 0$ and $p_{sR} = 0$). CNFET failure model presented in [15] only considers open defects that are due to CNT density variations and the application of a m-CNT removal process in which all m-CNTs are eliminated and maybe also some s-CNTs are removed ($p_{mR} = 1$ and $p_{sR} = 0$ or $p_{sR} \neq 0$). Our model does not consider CNT density variations (a uniform CNT density is assumed) but it is accurate when m-CNTs are not removed ($p_{mR} = 0$ and $p_{sR} = 0$) as well as and ideal ($p_{mR} = 1$ and $p_{sR} = 0$) or non-ideal m-CNT removal ($p_{mR} = 1$ or $p_{mR} < 1$ and $p_{sR} = 0$ or $p_{sR} \neq 0$) process is applied.

5.1. Probability of CNFET failure: derivation of the model

Let us consider that a CNT has a probability of being metallic (p_m) and of being semiconducting ($p_s = 1 - p_m$). Let us further consider that the probability of removal during the m-CNT removal process is p_{sR} for s-CNTs and p_{mR} for m-CNTs. For an N-tube CNFET, the transistor is short when there are one or more m-CNTs. In other words, the device is only "not short" when all the CNTs are semiconducting. As in [32], we can derive the probability of a transistor's being short (p_{short}) from the probability of all CNTs being semiconducting

$$1 - p_{short_{Ntubes}} = (1 - p_{short_{1tube}})^N = (1 - (p_m(1 - p_{mR})))^N \quad (5)$$

Then,

$$p_{short_{Ntubes}} = 1 - (1 - (p_m(1 - p_{mR})))^N \quad (6)$$

In contrast, an open occurs when all the CNTs are removed. Based on [15], the probability of an open for an N-tube CNFET can be calculated as

$$p_{open_{Ntubes}} = (p_m p_{mR} + p_s p_{sR})^N \quad (7)$$

Therefore, the overall probability of failure of a single N-tube CNFET is given by

$$p_f = p_{short_{Ntubes}} + p_{open_{Ntubes}} \quad (8)$$

It should be noted that the reliability of CNFETs at the circuit level was studied in [38]. That study derives the probability of failure of a

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chip consisting of M transistors (i) when the M CNFETs are independent of each other (uncorrelated) and (ii) when some of the M CNFETs are correlated, that is, when they share the CNTs. If CNFETs are perfectly correlated, a circuit's probability of failure can be reduced.

Using Eq. (8), Fig. 5 shows the probability of CNFET failure vs. the average number of CNTs in the channel for the three m-CNT removal cases and for different p_m.

When m-CNTs are not eliminated, the probability of failure is the probability of a short. Note that it is quite high for all four m-CNT probabilities and that it increases as N and p_m increase (Fig. 5a) – i.e. the probability of failure for $p_m = 33\%$ rises above 0.9 when the average number of CNTs is more than 7. As noted, m-CNTs are thus the main cause of CNFET failure and so different options to deal with this "m-CNT problem" and decrease this high probability of short have been proposed. These include: (1) self-sorting m-CNT techniques [20], (2) selective etching of m-CNTs [22,24], (3) electrical burning of m-CNTs [21], and (4) metallic-CNT-tolerant design methodology (ACCNT) [39]. Shorts are also illustrated in Fig. 2(b). The black curves representing a very high I_{OFF} ($\sim 10^{-6}$ A) are shorts when one or more CNTs are metallic, while the green lines are shorts when all 7 CNTs are metallic. We have called these situations *partial – short* and *full – short*, respectively. A percentage of shorts as high as 94% can be obtained for the worst p_m case considered.

In contrast, in the case of an ideal m-CNT removal process, the p_f is the probability of an open. As shown in Fig. 5b, it is much lower than in the previous case and it exhibits the opposite behavior; it decreases as N becomes bigger. These opens can also be observed in Fig. 2(d) and they account for 0.07% of the samples.

When a non-ideal m-CNT removal technique is applied, two different behaviors can be observed. If we consider that all m-CNTs and some s-CNTs are removed ($p_{mR} = 100\%$ and p_{sR} = 10–40%), p_f is once again the probability of an open, as shown in Fig. 5c. This is similar to Fig. 5b, but presents higher values. In contrast, if a small portion of the m-CNTs survives ($p_{mR} = 99.99\%$ and p_{sR} = 1–40%), the probability of CNFET failure is the sum of p_{open} and p_{short} and it behaves strangely (Fig. 5d), declining sharply at the outset, before gradually rising back up. This is because at first the probability of an open is the dominant component, but, as the average number of CNTs increases, the probability of a short becomes dominant. It should moreover be noted that the probabilities of failure are different for a single p_m for

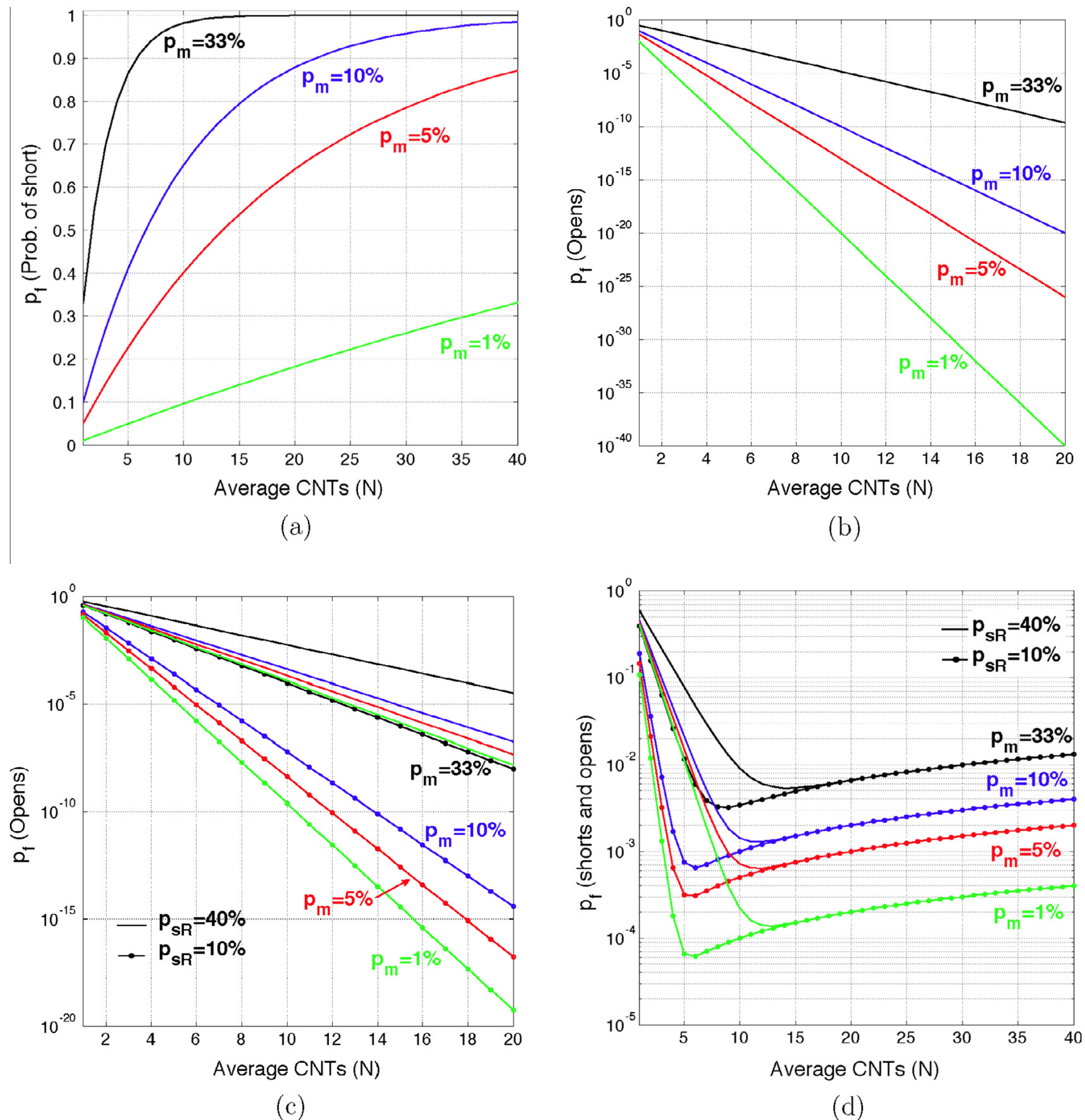

Fig. 5. Probability of CNFET failure vs. average CNTs: (a) when no m-CNTs are removed; (b) when an ideal m-CNT removal process is considered; and (c and d) when a non-ideal m-CNT removal process is applied for $p_{mR} = 100\%$ and $p_{mR} = 99.99\%$, respectively.

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the two p_{sR} considered when N is small, but that they become identical as of a given value of N – i.e. for large N the probability of CNFET failure is dominated by the probability of short and it is independent of p_{sR}. Finally, it is worth noting that there is an optimum average number of CNTs to minimize the probability of failure in this last case.

6. Conclusion

This paper presents a complete reliability and variability study of carbon nanotube technology in the presence of CNFET manufacturing imperfections, giving a realistic view of the challenges these devices face today and evaluating the impact of these manufacturing issues on CNFET performance.

First, we introduced a methodology to analyze the main sources of variability in the CNFET manufacturing process, such as CNT diameter, doping and density fluctuations, and the presence of metallic CNTs. This method, which is based on a MATLAB script and the Stanford CNFET HSPICE model, is able to simulate heterogeneous (non-ideal) transistors, that is, CNFETs with different numbers of tubes that have different diameters, are not uniformly spaced, have different source/drain doping levels, and, most importantly, are made up not only of semiconducting CNTs but also metallic ones, this latter factor being one of the biggest challenges in CNFET technology today. We performed 10000 Monte Carlo simulations for an n-type CNFET ($N = 7$), considering different m-CNT removal scenarios and m-CNT probabilities (p_m): (i) when no removal technique is used; (ii) when an ideal removal method is considered; and (iii) when a non-ideal m-CNT removal process is applied.

Furthermore, a model for analyzing CNFET failures was derived. The model takes into account both opens and shorts and is accurate for different m-CNT removal scenarios.

From the point of view of reliability, the presence of m-CNTs and variations in the CNT count are the main causes of failure. Metallic CNTs must be eliminated because they result in shorts. In 1-tube CNFETs, there is a 1% probability of a short with just a 1% probability of m-CNTs; this probability grows higher in multichannel CNFETs. Different m-CNT removal techniques are used to reduce the probability of a CNFET short, but their use increases the variations in CNT count; in other words, by reducing the average number of CNTs in the transistor, they increase the probability of an open. If a non-ideal m-CNT removal process is used, some s-CNTs are eliminated and a small percentage of m-CNTs survives; there is a unique optimum average number of CNTs. It should be noted that for the best case considered ($p_m = 1\%$, $p_{mR} = 99.99\%$, and $p_{sR} = 10\%$), the minimum probability of CNFET failure was in the order of 10^{-4}, which is very high for VLSI systems. If an ideal m-CNT removal process could be used, between 5 and 20 CNTs would be required to ensure a $p_f = 10^{-10}$ and, thus, a yield of $\sim$100%.

From the point of view of variability, when an ideal m-CNT removal process was considered, I_{ON} and I_{ON}/I_{OFF} parameters were highly affected by count variations, yielding variability values ($3\sigma/\mu$) of 47.49% and 185.67%, respectively, for the worst-case ($p_m = 33\%$) scenario. Threshold voltage showed a more moderate fluctuation of about 12% and remained almost constant for all p_m cases. It should be pointed out that CNFETs in which all m-CNTs are removed have a high I_{ON}/I_{OFF} ratio of $\sim 10^6$, but the presence of m-CNTs in the transistor severely degrades it.

Today, great efforts are being made to improve CNFET device processing and to optimize CNFET circuit design techniques. Only in this way can CNT technology become one of the most viable options for minimum-size transistors of less than 7 nm, which are expected to be produced by the early 2020s.

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