

Assessment of Light Flicker Mitigation using Shunt Compensators

Suman Poudel and Neville R. Watson

Abstract — The main objective of this paper is to compare the relative effectiveness of shunt compensators in mitigating light flicker caused by arc furnace. A test system comprising an arc furnace model built in PSCAD/EMTDC is simulated with and without the Static Var Compensator (SVC) and Static Synchronous Compensator (STATCOM). Compensation characteristics of the devices are measured in terms of flicker severity indices (P_{st}) using IEC compliant flickermeter model developed in PSCAD/EMTDC. The simulation results demonstrate that the STATCOM has superior flicker reduction capacity than the SVC due to its inherently faster response.

Index Terms—Arc furnace, power-factor compensation, flickermeter, flicker, SVC, STATCOM.

I. INTRODUCTION

A MODERN power system is a complicated network connecting a large number of electrical equipment. Heavy industries like steel mills connected at the local grid in a power system consume a large amount of power, which fluctuates with time. They have large and highly non-linear arc furnace load. The current drawn by such load is rapidly varying during the melting process. The rapid variations of current produce voltages drop in the system impedance of the AC system resulting in fluctuating voltage at points of common coupling (PCC). If the voltage fluctuates within the frequency range of 0.5-35 Hz then this causes variation in the illumination intensity of an electric light. This variation of an electric light is called light flicker. Although observed mainly in incandescent lamps, on rare occasions fluorescent lamps also exhibit light flicker.

Light flicker can be very annoying and hazardous if allowed to persist for a long time, hence the interest in its mitigation. SVC and STATCOM are two devices used for power-factor correction of arc furnace loads. Although their primary function is for power-factor correction their secondary benefit, and the subject of this paper, is their ability to reduce light flicker.

First of all, the International Electrotechnical Commission (IEC) flickermeter model, built in PSCAD/EMTDC, is tested for compliance to verify it can accurately quantify light flicker [1]. The SVC and STATCOM are implemented in a simply

The authors are with the Electrical and Computer Engineering, University of Canterbury, New Zealand.

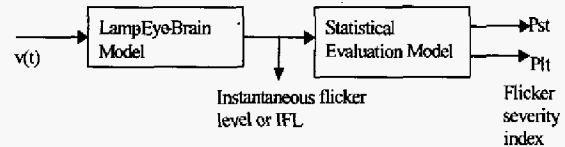


Figure 1 IEC flickermeter model

test system with an arc furnace load model built in PSCAD/EMTDC [2]. The SVC and STATCOM reduces the light flicker severity by reducing the voltage fluctuations by appropriate injection of reactive power.

II. IEC FLICKERMETER

The flickermeter is a device that can produce an output representative of human visual sensation by detecting any variation in input voltage. It must be able to represent the dynamic characteristics of the lamp and the non-linear frequency characteristics of the eye-brain chain. The flickermeter built in PSCAD/EMTDC uses this understanding of lamp-eye-brain model to simulate the flicker levels that causes irritation to eye.

Figure 1 shows the main components of a flickermeter [3]. The first component describes the lamp-eye-brain model to represent human sensitivity to illumination intensity. The output from the lamp-eye-brain model is the representation of flicker sensation and is called the instantaneous flicker level or IFL. It is measured in unit of perceptibility (pu). IFL is directly proportional to voltage variations. The second component is the quantitative statistical evaluation of the output from the lamp-eye-brain model. The output from this block is called flicker severity index or P_{st} and it is the true representation of the degree of human eye irritation. A P_{st} value is based on a short-term observation period of 10 minutes and is given by the following equation [4]:

$$P_{st} = \sqrt{0.0314P_{0.1} + 0.0525P_1 + 0.0657P_3 + 0.28P_{10} + 0.08P_{50}} \quad (1)$$

where $P_{0.1}$, P_1 , P_3 , P_{10} , and P_{50} are the percentiles or gauge points representing the instantaneous flicker level exceeded for 0.1%, 1%, 3%, 10% and 50% of the time (10 minutes observation time).

A. Compliance Test

IEC has specified a set of sinusoidal and rectangular input voltage flicker test signals for a 230V, 50Hz system to test the compliance of the flickermeter [4]. The compliance is proven if the maximum IFL lies within $\pm 10\%$ of the reference value of one unit of perceptibility. Compliance is also proven if P_{st} lies within $\pm 5\%$ of one unit of perceptibility. The range of input values of test signals at frequencies between 0.5 to 33.33Hz is given in references [4]-[5].

A test circuit was built in PSCAD/EMTDC along with IEC flickermeter model. The rectangular and sinusoidal test signals are generated using the test circuit and applied at the input of custom flickermeter. Figure 2 and 3 shows the test input signals while Figures 4 and 5 shows the compliance results of flickermeter model.

The steady-state part of the simulation results in Figures 4 and 5 clearly shows that the IFL and P_{st} lie within their respective prescribed ranges.

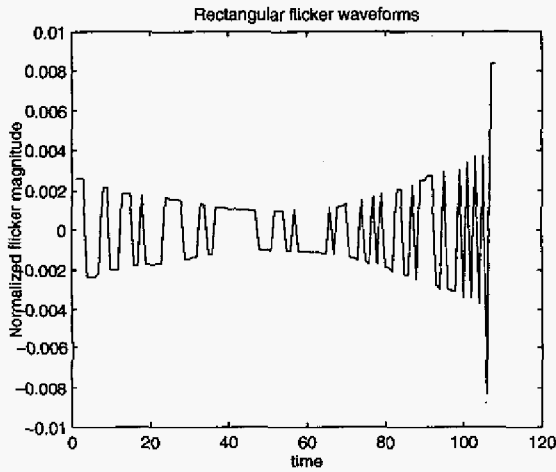


Figure 2 Rectangular flicker input waveforms

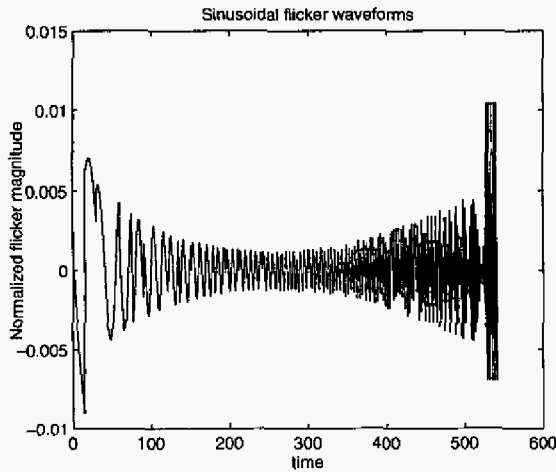


Figure 3 Sinusoidal flicker input waveform

III. TEST SYSTEM FOR LIGHT FLICKER MITIGATION

Figure 6 represents a single line diagram of the studied power system network. It has an arc furnace, lighting load and compensator connected at the PCC. Lighting load is replaced by flickermeter to measure P_{st} at this point. The arc furnace load is supplied by a medium to low voltage furnace transformer. A high voltage to medium voltage transformer is connected to the supply source. The test system is divided into two parts; test circuit without the compensators and the test circuit with a suitably sized SVC and STATCOM at the PCC.

The test system consists of two transformers, an arc furnace load (PSCAD/EMTDC model) and a source modeled by a Thevenin equivalent source having a base MVA and base voltage of 200 MVA and 138 kV (line-to-line) respectively. The Thevenin equivalent source impedance is $(0.025+j0.208)$ p.u. /phase. At the PCC the system impedance is larger due to the inclusion of 150 MVA (base value of transformer for

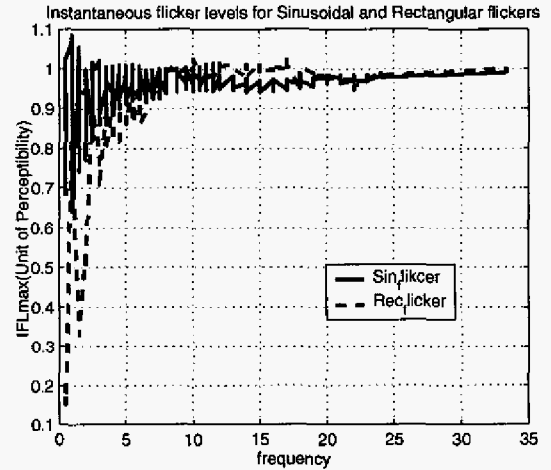


Figure 4 IFL for sinusoidal flicker and rectangular flicker.

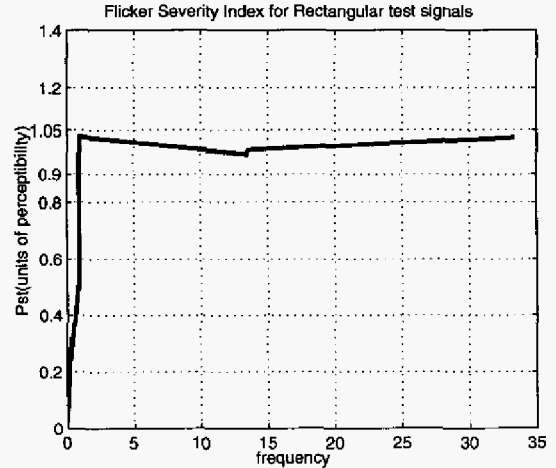


Figure 5 P_{st} for rectangular test signal.

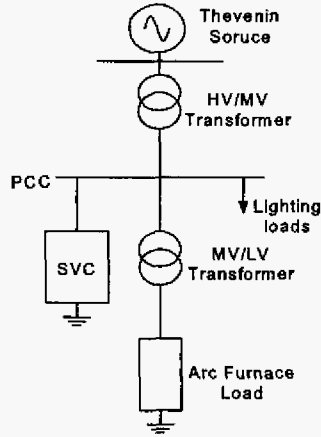


Figure 6 Single line diagram of test system

calculating per unit values), 138/15 kV transformer. Its leakage reactance is 10%.

The short circuit capacity of the Thevenin source is calculated to be 317.4 MVA per phase. Another 100 MVA (base value of transformer for calculating its per unit value) transformer steps down 15 kV to 0.9 kV (line-to-line) to suit the Electric Arc Furnace (EAF) operating voltage. A small cable reactance of 1.57×10^{-3} (Ohm) is included between transformer and arc furnace electrodes. The strength of the source is weaker at the PCC than the source terminal.

Figure 7 shows a simulation result for the real and reactive power requirements of a three-phase arc furnace load at the PCC before any shunt compensators are connected. It can be seen that both the real and reactive power varies randomly for the whole 10 seconds simulation. Also evident are the three stages in melting process.

Figure 8 shows the three phases currents and the lower figure in Figure 8 shows the expanded version of these currents with limited time scale. In fact these highly fluctuating currents are responsible for the voltage fluctuation and hence light flicker [6]. Figure 9 shows flicker severity index due to fluctuating current in phase A. It should be noted that the initial transient in P_{st} should be ignored as an artifact of the algorithm used. There are two initialization transients, the initialization transient of the electrical network and that of the flickermeter itself. To minimize spurious values at the start (and to have sufficient samples) the flickermeter has a time delay before updating its output. Then after this it takes another few seconds to settle. This results in a constant P_{st} of 10 for 3 s before jumping up then settling.

P_{st} level is well above the recommended level of one, sufficient enough to inflict light flicker [3].

IV. SVC COMPENSATION

In this paper it is shown that fixed capacitor, thyristor controlled reactor (FC-TCR) can be very useful in mitigating

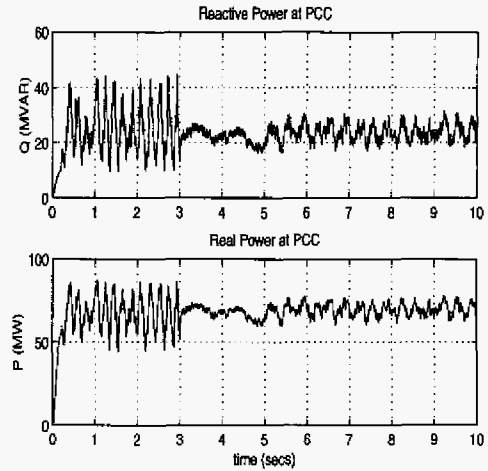


Figure 7 Real and Reactive Power demand of load at PCC

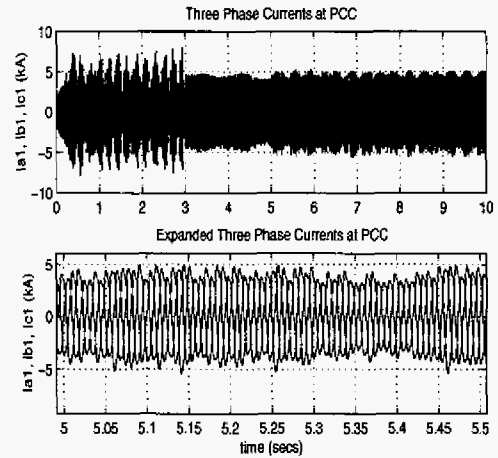


Figure 8 Three-phase currents at PCC

light flicker. FC-TCR has a fixed capacitor in parallel with a thyristor-controlled reactor. It is assumed that the compensator is a variable susceptance with no resistive component, as it draws negligible real power from the network. The reactive power is given by [7]:

$$Q_{svc} = -|V_{pcc}|^2 B_{svc} \quad (2)$$

where

V_{pcc} = Voltage at PCC.

$B_{svc} = (B_c + B_{TCR})$ = Equivalent Susceptance of capacitor and inductor.

Equivalent susceptance of the SVC depends on the susceptance of TCR (B_{TCR}) and capacitive susceptance (B_c) and it is given by the following equation [8]:

$$B_{TCR}(\alpha) = B_{\max} \left(1 - \frac{2\alpha}{\pi} - \frac{1}{\pi} \sin 2(\alpha) \right) \quad (3)$$

where

$$B_{\max} = \frac{1}{\omega L} \quad (4)$$

Equations (2)-(4) suggest that the maximum value of susceptance is obtainable with firing angle alpha at 180 degrees. Since fundamental reactive current of TCR is directly proportional to the B_{TCR} it is important that the susceptance is controlled appropriately by a robust control system to supply the required amount of leading reactive power at the PCC.

The reactive power compensation ability of SVC is determined by the size of the inductive and capacitive elements. The rating of capacitance and TCR inductance is calculated based on the simulation result of Figure 10 where

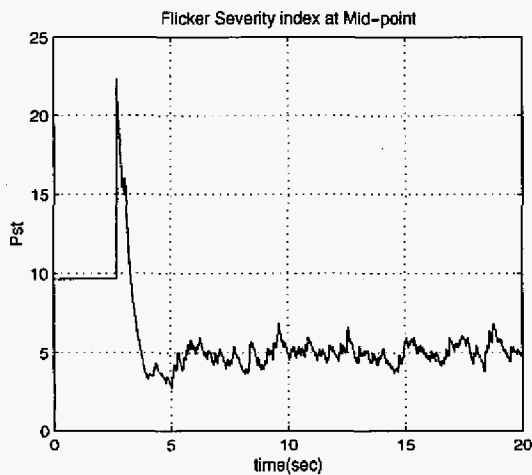


Figure 9 Flicker Severity Index before compensation

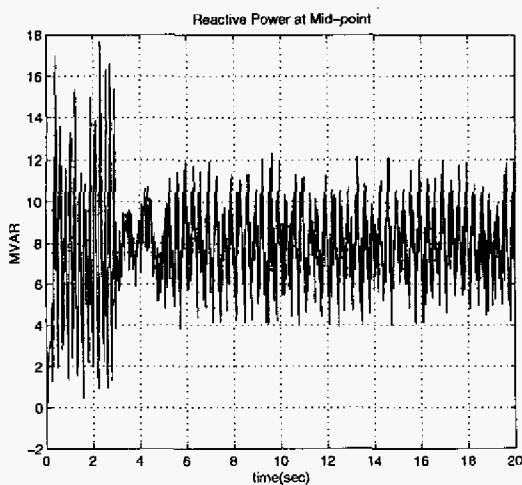


Figure 10 Reactive power measurement at mid-point (PCC)

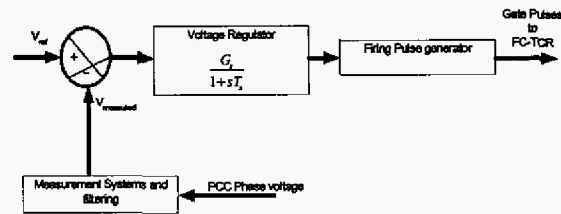


Figure 11 SVC Control System

the required maximum reactive power fluctuates between 4 MVAR to 12 MVAR/phase. The value of capacitance and inductance and is found to be 848.88 μ F and 0.119 H.

The SVC has three core control system modules viz., measurement system, voltage regulator and a firing pulse generation. Figure 11 shows the block diagram of the control system for SVC.

The PCC voltage is passed through a series of low pass and notch filters (at 75 Hz, 50 Hz and 100 Hz) to insure that the measured RMS voltage remains free of any distortion or ripples. The filtered voltage is compared with a reference voltage, which can be varied between 0.95 p.u. and 1.05 p.u ($\pm 5\%$ of nominal phase voltage). The error signal is used as the input to the voltage regulator, which processes the input error signal and generates a susceptance (reactance) order as an output. The output is proportional to the required reactive power compensation and is a function of firing angle (α). Firing pulse generator processes the input susceptance order and generates the required firing pulses for the thyristors of the TCR. Figure 12 shows the effect of SVC control on P_{st} level for 20 seconds simulation.

P_{st} level has marginally reduced here contrary to its

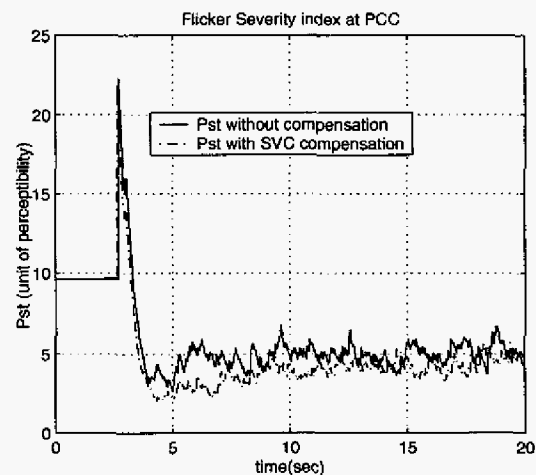


Figure 12 P_{st} level after compensation

maximum reduction capability by factor of two [6]. This is due to the slow response of controller to the fast changes in the reactive power requirement of the load.

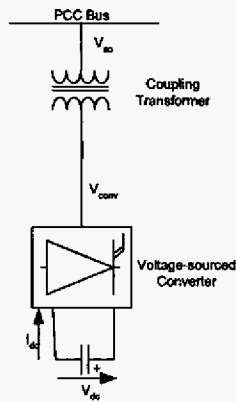


Figure 13 Schematics for STATCOM

V. STATCOM COMPENSATION

STATCOM consists of three-phase bridge converter with power electronic switches that have turn OFF capability. In its simplest configuration it has capacitor on its DC side, VSC in the middle and a coupling transformer on the AC side. SVC in Figure 6 is replaced by STATCOM to compensate the reactive power requirement of the arc furnace load. Figure 13 shows a schematic representation of a power system network with STATCOM connected at the PCC for flicker reduction.

The STATCOM provides reactive power compensation through the manipulation of the VSC terminal voltage (V_{conv}). When V_{conv} is greater than the AC system voltage at the PCC the STATCOM appears capacitive and supplies reactive power. The converse is also true with the STATCOM appearing inductive when V_{conv} is less than V_{ac} . If the amplitude of the output voltage is same as that of AC system voltage then the net reactive power exchange is zero. Although the real power exchange under steady state is approximately zero, transiently it can supply/absorb real power.

The STATCOM is connected at the PCC by Y-Y transformer. The coupling transformer leakage reactance is chosen to be 10%. The DC capacitor value is 1000 μ F, which provides energy storage capacity for the STATCOM. The STATCOM is controlled to provide only ± 15 MVAR of reactive power whereas the other 20 MVAR of power is provided by a fixed capacitor on the AC side of the transformer. The capacitor acts as a reactive power compensator at fundamental frequency but provides a low impedance path for higher frequencies.

PWM switching strategies is used to control the VSC valves. PWM uses a carrier frequency, which is compared to a control signal (sinusoidal) to determine the switching instances for the converter. The carrier frequency is kept at 39 times the fundamental to minimize excess harmonic effects. Figures 14 and 15 shows the block diagrams of an AC and DC control loops for STATCOM. The magnitude and angle order obtained from the two loops are used to generate a sinusoidal control signal, which is compared with the carrier frequency.

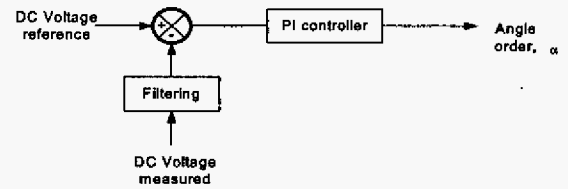


Figure 14 DC Voltage Control

Figure 15 shows a block diagram of control loop for the generation of firing pulses. The magnitude of output voltage and hence the reactive power is controlled by varying the amplitude of control signal, which in turn depends on magnitude order. Since the system is designed to compensate reactive power only the angle order is made as small as possible to replenish the small amount of converter losses.

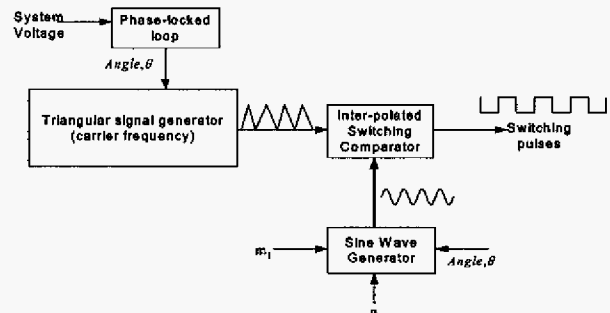


Figure 15 Control system for the generation of firing pulses

The output voltage for phase A is shown in Figure 16. The lower expanded scale depicts a very low amplitude modulation.

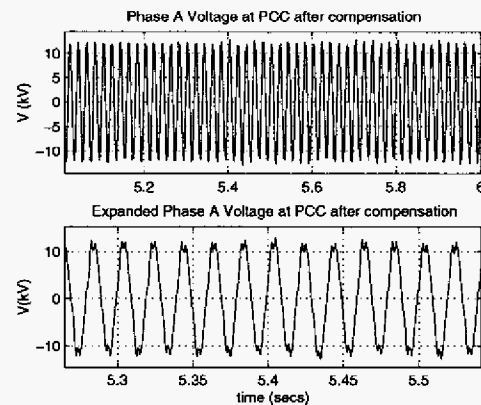


Figure 16 Voltage at phase A

This means less voltage fluctuation and hence the flicker severity index must also be reduced significantly [9]. Figure 17 shows the P_{st} reduced to almost half after application of STATCOM compensation. Figure 17 shows a comparison with Figure 12 to see the difference between STATCOM and SVC compensation.

VI. CONCLUSION

Validated of the compliance of a PSCAD/EMTDC model of the IEC flickermeter, for light flicker measurement, has been performed. Both IFL and P_{st} were within the prescribed ranges specified by IEC standard. This flickermeter has then been used for a simple comparison of the light flicker mitigation performance assessment of an SVC and STATCOM. The simple test system was arbitrary and somewhat harsh as the flicker levels are higher than normally experienced due to the absence of the moderating influence of other loads, particularly motor loads. Nevertheless it has demonstrated the superior light flicker mitigation capability of the STATCOM compared to an SVC.

VII. ACKNOWLEDGEMENTS

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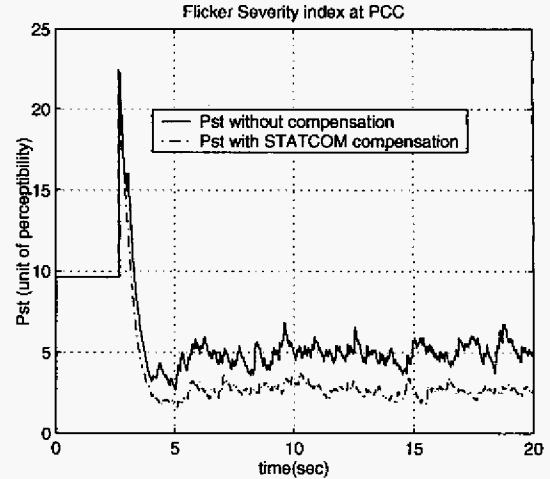


Figure 17 Flicker severity index after compensation