Analog Integr Circ Sig Process (2012) 70:123–132
DOI 10.1007/s10470-011-9640-7

Power and area efficient MOSFET-C filter for very low frequency applications

Armin Tajalli · Yusuf Leblebici

Received: 17 January 2011 / Revised: 21 March 2011 / Accepted: 1 April 2011 / Published online: 17 April 2011

Abstract New circuit design techniques for implementing very high-valued resistors are presented, significantly improving power and area efficiency of analog front-end signal processing in ultra-low power biomedical systems. Ranging in value from few hundreds of MΩ to few hundreds of GΩ, the proposed floating resistors occupy a very small area, and produce accurately tunable characteristics. Using this approach, a low-pass MOSFET-C filter with tunable cutoff frequency (f_C = 20 Hz–184 kHz) has been implemented in a conventional 0.18 μm CMOS technology. Occupying 0.045 mm^2/pole, the power consumption of this filter is 540 pW/Hz/pole with a measured IMFDR of 70 dB.

Keywords CMOS integrated circuits · Continuous-time filter · High-valued resistance · Low-power · MOSFET-C filter · Programmable filter · Subthreshold · Weak inversion · Widely tunable circuits

1 Introduction

Analog front-end data acquisition and signal processing are critically important functions in modern biomedical systems, such as in biopotential capture and neural recording [1–4]. Figure 1 depicts a conceptual data acquisition chain for biomedical systems. Based on this topology, the biomedical signals are converted to electrical signals by parallel transducers; the electrical signals are then amplified by a low-noise amplifier. The next step will be to convert the analog signals to digital signals (analog-to-digital converter) after filtering to be further analyzed by the digital signal processors. Performance parameters such as linearity, gain and noise, as well as system specifications such as power dissipation and silicon area, are the main issues in design of analog front-end for this type of applications. Because of very limited energy budget in such battery operated or battery less systems [5], extremely power efficient circuit design techniques must be employed.

Depending on application, the bandwidth of input signal ranges from below 1 Hz to few kHz [6]. For example, signal bandwidth for Electroencephalography (EEG), Electrooculography (EOG), and Electrocardiography (ECG) applications are in the range of 0.5–40 Hz, DC to 10 Hz, and 0.05–100 Hz, respectively. Therefore, versatile amplification and filtering front-end circuits with very low operating frequencies are very desirable.

In [1], capacitance and transconductance scaling techniques have been introduced to implement a low-pass 2.4 Hz filter with 690 nW/Hz/pole power dissipation and 0.16 mm^2/pole area in 1 μm CMOS. To generate a very large time constant, transconductance-transimpedance technique has been used in [2]. An integrator with a time constant of 0.2–10 s has been implemented in 0.8 μm CMOS, consuming 230 nW and occupying 0.1 mm^2. To implement low bandwidth amplification stages, a very high-valued pseudoresistor has been introduced in [3]. In this pseudoresistor topology, each transistor which occupies 16 μm^2, is biased in weak inversion to exhibit a very high resistivity. While highly nonlinear, it shows a

A. Tajalli (✉) · Y. Leblebici
Microelectronic Systems Laboratory (LSM), Ecole Polytechnic Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland
e-mail: armin.tajalli@epfl.ch

Y. Leblebici
e-mail: yusuf.leblebici@epfl.ch

Present Address:
A. Tajalli
Kandou Technologies Inc., 1015 Lausanne, Switzerland

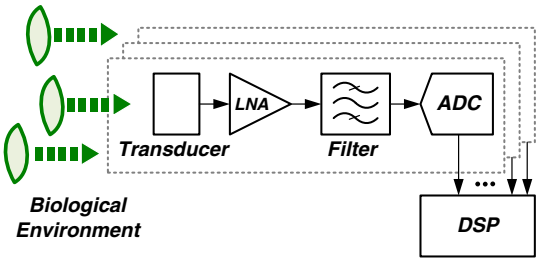

Fig. 1 A conceptual biomedical data acquisition system

resistivity of as high as $\approx 10^{12}\,\Omega$. To reach to the same range of resistivity, in [6] a pseudoresistance combined of NMOS and PMOS devices with better linearity performance has been suggested.

As can be seen, very high resistivity devices are critical components for implementing power and area efficient filters at very low frequencies. In this article some techniques for implementing very high-valued resistors (HVRs) will be presented and used to realize a low frequency MOSFET-C filter [7, 8]. Having a cutoff frequency of as low as 20 Hz, the proposed low-pass filter consumes only 540 pW/Hz/pole and occupies 0.045 mm^2/pole in 0.18 μm CMOS.

2 High-valued resistance

One of the main concerns in the design of very low frequency circuits is the size of passive components [9]. Large passive components can be very expensive in terms of silicon area. Meanwhile, when the size of a component increases, the parasitic elements associated with this device can affect the circuit performance. Therefore, compact and high-valued resistors are very desirable for implementing low-frequency filters. This Section explains step-by-step the topology of the proposed HVRs.

2.1 Basic HVR with extended swing

Triode MOS devices have been widely used in design of MOSFET-C filters [10] (Fig. 2(a)). However, the resistivity of such devices is generally limited to few tens of MΩ with a reasonable area occupation. To implement compact and high-valued resistors especially for biomedical applications, several techniques have been proposed in literature [3, 6, 11–14]. The technique that will be discussed here is based on a simple topology first used to implement logic circuits [15]. Using this technique, resistors with values as high as 20 GΩ based on small size devices have been fabricated and tested [7].

Previously, it has been demonstrated by the authors that connecting the bulk of a PMOS transistor to its drain will extend the resistivity range of device compared to the

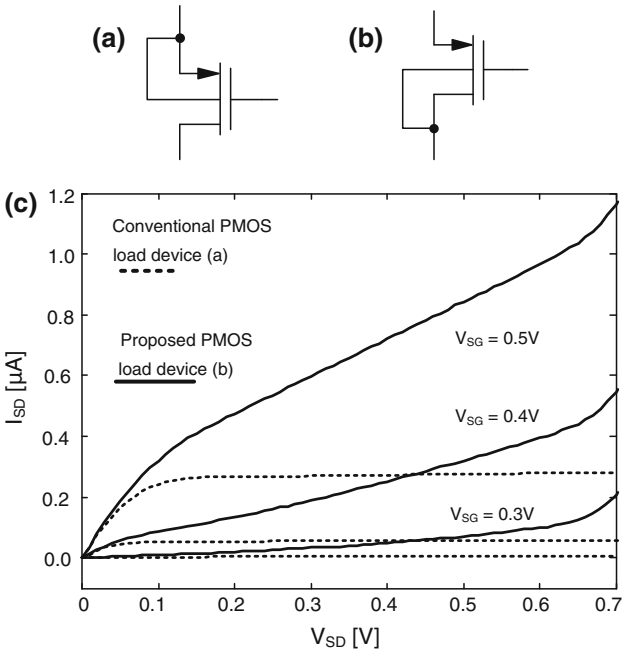

Fig. 2 High-valued resistance for implementing subthreshold source-coupled logic [15]

conventional bulk-source connected configuration (Fig. 2(b)) [7]. As shown in Fig. 2(c), while the I/V characteristic of the conventional topology saturates for V_{SD} values larger than few U_T (U_T is the thermodynamic voltage), with the modified topology the resistivity range extends to few hundreds of mV. Ignoring the current of the forward bulk-source PN junction, the equivalent resistance of this topology can be calculated by

$$R_{SD} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\right)^{-1} = \frac{n_p U_T}{I_{SD}} \times \left(\frac{e^{V_{SD}/U_T} - 1}{(n_p - 1)e^{V_{SD}/U_T} + 1}\right) \quad (1)$$

which is obviously very non-linear (here, n_p is the subthreshold slope factor of the PMOS device). However it can be shown that as long as the device is in subthreshold regime, the linearity remains fairly independent to the absolute value of resistance. Using Taylor expansion for (1):

$$\begin{aligned} R_{SD} &= R_0 \cdot e^{-\frac{V_{SD}}{U_T}\cdot\frac{n_p-1}{n_p}} \\ &\approx R_0 \cdot \left(1 - \alpha \cdot \frac{V_{SD}}{U_T} + \frac{\alpha}{2} \cdot \left(\frac{V_{SD}}{U_T}\right)^2\right) \end{aligned} \quad (2)$$

where:

$$\alpha = \frac{n_p}{n_p - 1} \quad (3)$$

indicates that the nonlinear part of the I/V characteristics depends only on V_{SD}/U_T, and hence the nonlinear component remains the same for different values of bias current or

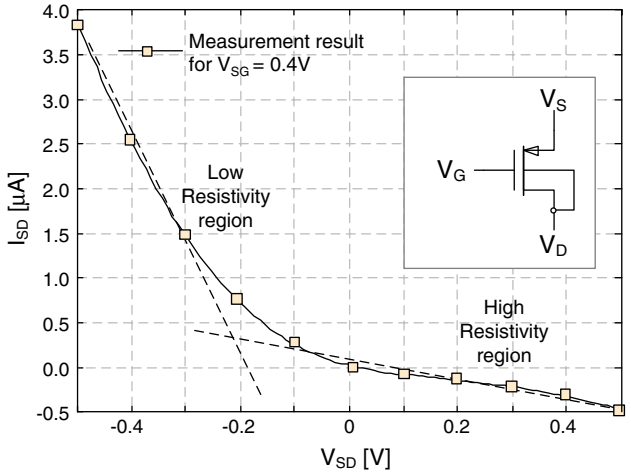

Fig. 3 Measured I/V characteristics of the device shown in Fig. 2(b) for positive and negative V_{SD}

V_{SG}. Here, R_0 stands for the resistivity of the circuit when V_{SD} = 0 V. Based on (2), nonlinearity depends weakly on the biasing condition only through n_p.

The other important aspect of the device shown in Fig. 2(b) is that when the drain voltage of this component becomes larger than the source voltage, then the drain and source of the device will be exchanged and the bulk is connected to the source node. Therefore, the resistivity of the device will quickly switch from a very high value to a very low value similar to a PN junction. Depicted in Fig. 3, based on measurement results in 0.18 µm CMOS, the device switches from subthreshold to strong inversion by changing the polarity of the source-drain voltage.

As far as the voltage swing across the resistor shown in 2(b) is less than 500 mV, the forward biased diode of the source-bulk junction draws very small amount of current and it has a negligible effect on the I/V characteristics, and power dissipation of the circuit.

2.2 Floating HVR

To compensate the asymmetric I/V characteristics of the simple devices discussed above, one can use two back-to-back equal-sized devices to implement a symmetric and floating pseudoresistor. The schematic of such a device is shown in Fig. 4.

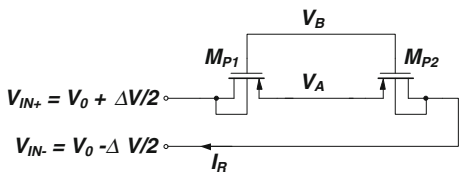

Fig. 4 Implementing floating HVR using two equal-sized back-to-back bulk-drain shorted PMOS devices. $V_C = V_A - V_B$ can be adjusted for controlling the device resistivity

Regarding Fig. 4, since the two transistors in series are not linear devices, $V_A \neq (V_{IN+} + V_{IN-})/2$. Using the EKV model [16], it can be shown that:

$$V_A = V_0 - U_T \ln\left(\frac{\cosh\left(\frac{\Delta V}{2n_p U_T}(n_p - 1)\right)}{\cosh\frac{\Delta V}{2n_p U_T}}\right) \tag{4}$$

Therefore, V_A depends on input voltage swing, ΔV. The voltage at node V_A exhibits a "V-shape" characteristic with respect to ΔV. The minimum value occurs at $\Delta V = 0$ V, and then increases by increasing $|\Delta V|$. Knowing the value of ΔV, it is possible to calculate the current flow through MP1 and MP2:

$$I_R = I_0 e^{\frac{V_0 - V_B}{n_p U_T}} e^{-\frac{\Delta V}{2n_p U_T}}\left(1 - e^{\frac{\Delta V}{2U_T}} \cdot \frac{\cosh\frac{\Delta V}{2n_p U_T}}{\cosh\left(\frac{\Delta V}{2n_p U_T}(n_p - 1)\right)}\right). \tag{5}$$

Based on this, the circuit shown in Fig. 4 achieves its maximum resistivity when $\Delta V = 0$ V, and then the resistivity drops when $|\Delta V|$ increases. If we generate V_B from V_A, for example using a level shifter, then the linearity can be improved. The reason is that when V_A increases with increasing $|\Delta V|$ as can be deduced from (4), the drop in resistivity will be canceled out partially by reduction of V_{SG} of the PMOS devices. In this case, the maximum value of the resistance will be no longer at $|\Delta V| = 0$ V, but at two different points symmetrically placed with respect to the $|\Delta V| = 0$ V.

Based on this discussion, it is possible to combine the two possible topologies to improve the linearity. For example, a series connection of the two circuits like the one shown in Fig. 5 could be used to significantly improve the linearity. In this circuit, MN has been used to generate the gate voltage of MP1–MP2, V_B, with respect to V_A as a level shifter circuit. Transistors MP1–MP2 are put in series to MP3–MP4 which are biased with a constant gate voltage. The resistivity of this circuit can be adjusted through the bias current of the level shifter circuit, I_C. By increasing this current, the source-gate voltage of MP1–MP2 increases, and hence the resistivity decreases. Based on simulation results shown in Fig. 5, the nonlinearity of this pseudoresistance is about 7% for 2 V peak-to-peak voltage swing. Using more transistors in series with appropriate gate bias voltages can provide HVRs with better linearity performance within a still compact area.

2.3 Extremely high-valued resistance

The analysis and discussion provided in Sect. 2.2 is based on the assumption that the devices are biased in inversion mode where $V_{SG} \geq 0$. If we reduce the gate source voltage

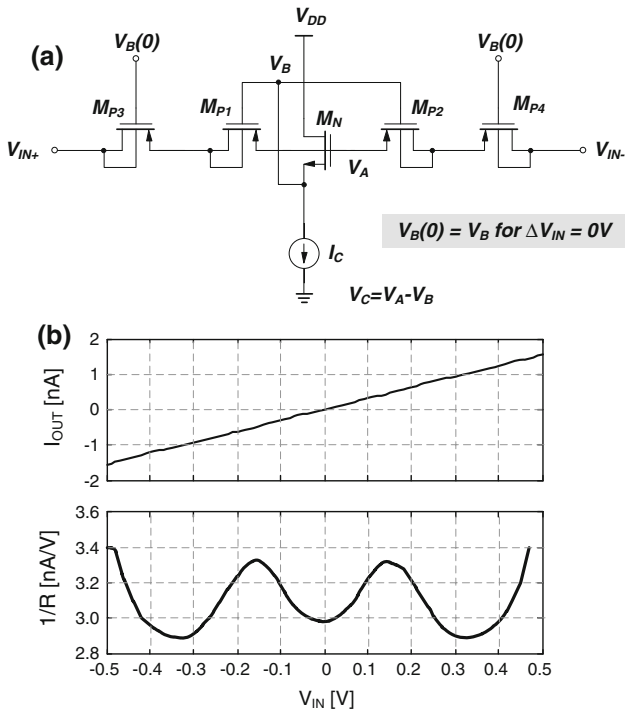

Fig. 5 **a** Modified HVR with improved linearity performance. **b** Simulated I/V characteristics of the proposed HVR. This figure also shows the variation on absolute value of the HVR in different voltage drops

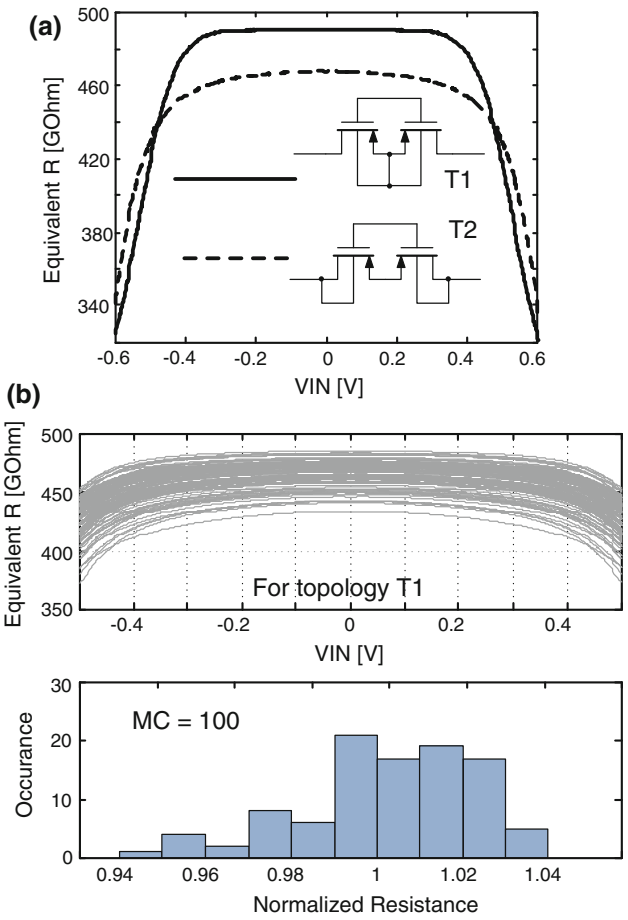

Fig. 6 **a** Extremely high-valued compact resistor with a good linearity performance. The equivalent resistance of both topologies are shown. **b** Variation on resistivity based on Monte Carlo Simulations (MC = 100). The Monte Carlo simulations are shown for the topology T1. Here, supply voltage and temperature are constant and a fixed voltage is applied to the gate of transistors

even further and make it negative, as shown in Fig. 6(a), it is possible to implement extremely high valued resistors with a fairly good linearity performance. This figure shows the resistivity of the circuit for two different configurations. Monte Carlo simulations have been performed to study the resistivity variation in this topology. As it is shown in Fig. 6(b), the resistivity variation based on MC = 100 simulations is only $\sigma = 2.2\%$. In the Monte Carlo simulation, mismatch and process variation for transistors is considered, while the supply voltage, temperature, and gate voltage of the devices are constant.

3 Tunable MOSFET-C filter design

Using the HVR topology introduced in Sect. 2, it is possible to implement very low frequency MOSFET-C filters. Wide tuning range associated with this HVR is especially interesting for implementing a versatile filter that can be used in different applications.

Figure 7 proposes a first order MOSFET-C filter that uses a variable resistance for adjusting its cutoff frequency. Here, a widely tunable resistance and a high-gain and robust OTA (operational transconductance amplifier) with scalable power consumption are the main building blocks to implement a wide tuning range MOSFET-C filter. To scale the circuit power consumption with respect to the filter cutoff frequency (f_c), it is necessary to change the power consumption of the amplifier (through $I_{B,OP}$) proportional to f_c (or inversely proportional to R). The circuit topologies introduced in Sect. 2 can be used to implement the required resistance in Fig. 7.

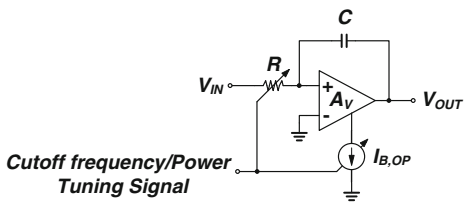

Fig. 7 Tunable active-RC (MOSFET-C) filter using a variable resistor. The power consumption of the amplifier needs to be scalable with respect to the filter cutoff frequency

3.1 Amplifier design

In this work a two stage amplifier topology has been utilized. Assuming that the dominant pole is at the output of the first stage of amplifier, then the unity gain-bandwidth (UGBW) of the amplifier will be:

$$UGBW \simeq g_{m1}/(2\pi C_C) \tag{6}$$

which is proportional to g_{m1} (transconductance of the input stage shown in Fig. 8(a)), and inversely proportional to the compensation capacitance (C_C). Assuming that the input devices are in subthreshold regime, then:

$$UGBW \simeq \frac{I_{SS}}{2nU_T} \cdot \frac{1}{2\pi C_C} \tag{7}$$

which is proportional to the bias current of the input stage of amplifier (I_{SS}). Meanwhile, to have a phase margin of at least 60° [17]:

$$f_{p,nd} \geq 3 \times UGBW \tag{8}$$

where, $f_{p,nd}$ is the non-dominant pole of the amplifier. The value of $f_{p,nd}$ is inversely proportional to the load resistance R_L. R_L is the equivalent load resistance of the amplifier and as calculated in (1), it can be adjusted by the bias current. It is assumed that the output resistance of OTA itself is much larger than R_L.

As illustrated in Fig. 8(a), a two stage amplifier topology has been utilized for this purpose. To achieve a phase margin of at least 60°, based on (8) it is necessary to have:

$$\frac{1}{3} \cdot \frac{C_C}{C_L + C_C} \geq \frac{g_{m1}}{G_L}. \tag{9}$$

Since the value of g_{m1} and $G_L = 1/R_L$ are both proportional to the bias current, by properly choosing the size of devices, the right hand side of (9) can be made bias current independent. Therefore, as long as the devices are in subthreshold regime, the stability of the circuit can be guaranteed. In this figure, R_C is implemented using NMOS devices to follow the variations of the bias current. Figure 8(b) shows the simulated gain and phase margin of the proposed amplifier for different bias currents ranging over five orders of magnitude.

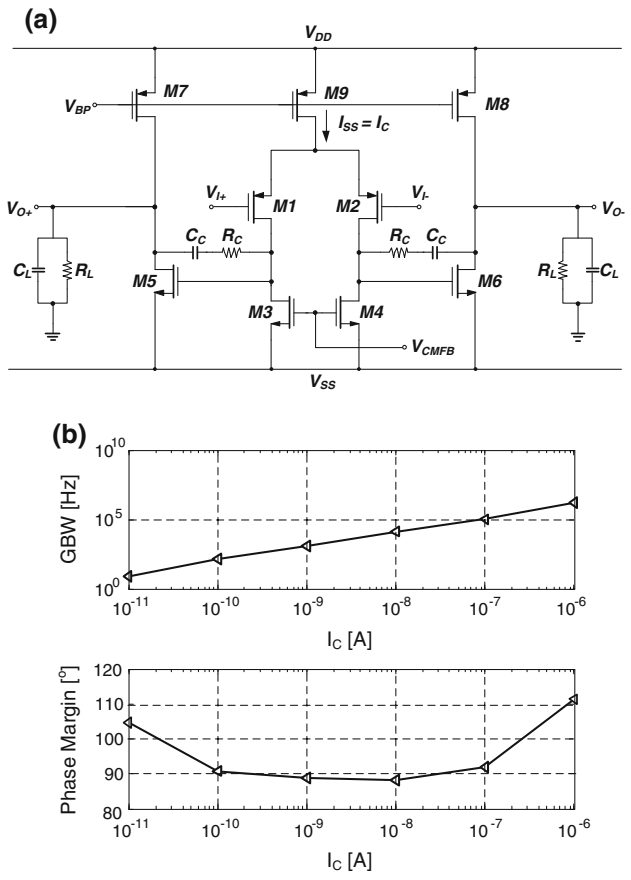

Fig. 8 **a** Circuit schematic of the amplifier. **b** Simulated unity gain bandwidth (UGBW) and phase margin of the amplifier for different current bias values. In this plot, I_C is the reference current value used to change the filter cutoff frequency ($I_C = I_{SS}$)

3.2 Dynamic range

The topology of the MOSFET-C filter shown in Fig. 7 is well suited for implementing constant dynamic range (DR) and widely adjustable filters. This property is mainly due to the almost constant *noise* and *linearity* performance of the filter over its tuning range. The total input referred noise power of the filter shown in Fig. 7 is:

$$v_{n,in}^2 = \gamma_F \cdot (k \cdot T/C) \tag{10}$$

in which γ_F indicates the circuit excess noise factor and depends on the topology of the amplifier, resistances, as well as to the filter frequency transfer function (here, k is Boltzmann's constant, T is the junction temperature in Kelvin, and C is the integration capacitance as shown in Fig. 7). Regarding (10) and assuming that γ_F is bias independent, then selecting a constant capacitor size results in constant total filter noise power for different cutoff frequencies.

On the other hand, based on (2) the linearity of the resistance introduced in Fig. 4 is independent of the bias current or V_{SG} and the dependence on V_{SD} is the same for different resistor values. Hence, as long as the devices are in subthreshold regime, the linearity performance of the resistance remains unchanged, as well.

4 Experimental results

Using the proposed floating resistor topology shown in Fig. 5, a second order MOSFET-C filter has been implemented. The topology of the filter is illustrated in Fig. 9. In

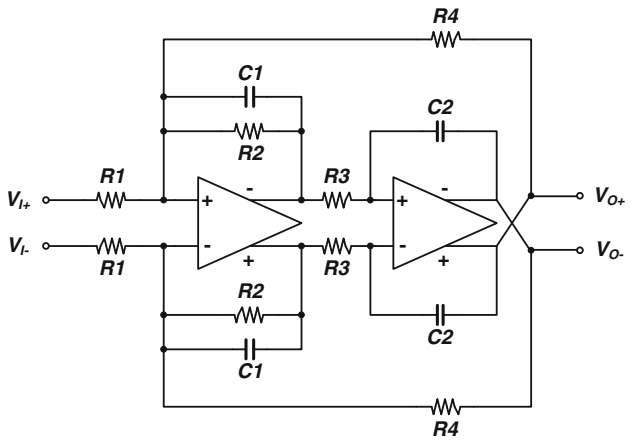

Fig. 9 A second order MOSFET-C filter. All resistors are implemented using the proposed floating resistor topology shown in Fig. 4(a). Quality factor of this filter can be tuned through R2 independent to the cutoff frequency. In this design, R1 = R3 = R4

this configuration, the cutoff frequency and the quality factor (Q) of the filter can be tuned independently by adjusting the value of the appropriate resistors [10].

Simulations show that the cutoff frequency of the filter can be adjusted from 10 Hz to 200 kHz. The linearity performance of the filter remains almost constant as long as the devices are in subthreshold. For high bias currents, when the devices are entering into medium and strong inversion, linearity improves slightly. For low input frequencies ($f_{in} \ll f_c$), the circuit transfer characteristic depends only on the ratio of resistors. Therefore, the nonlinearity of the resistors is not significant as long as they are well matched. For higher frequencies, when both capacitors and resistors are participating in constructing the output signal, then the nonlinearity of the resistors become important.

The chip photomicrograph of the filter is shown in Fig. 10. The proposed filter occupies a silicon area of 420 μm × 210 μm while using MiM capacitors. As shown in Fig. 10, the area of the proposed floating resistors can be compared with the size of other components in the circuit.

4.1 Frequency response

The measured frequency response of the filter versus input frequency controlling current (I_C) is shown in Fig. 11(a). In this measurement, the bias current of all the resistors as well as the bias current of amplifiers are scaling with respect to I_C. Depicted in this figure, the controlling current can be as low as $I_C = 100$ pA for $f_C \simeq 20$ Hz. This low cutoff frequency has been achieved using 2 pF filter capacitors. As a result, this topology shows to be very suitable for implementing very low frequency filters, using limited silicon area.

Figure 11(b) demonstrates the tunability of this filter in comparison to the simulation results. The measured cutoff frequency of the filter is $f_C = 20$ Hz–184 kHz which is slightly less than five decades. This very wide tuning range corresponds to the adjustability range of the proposed floating resistor which is shown in Fig. 12 based on measurement results. The measured frequency response shows a very good agreement with the simulation results. The small difference that can be seen between measurement and simulation results which is a relatively constant ratio over the entire range is mainly due to the difference between the capacitor values in the simulations and measurements. The difference between measurements and simulation results becomes more evident (about 50%) in very low cutoff frequencies mainly because of difficulty of precisely adjusting the controlling current. An internal current divider circuit has been employed to divide and external controlling current and produce the controlling current of the filter which loses its precision below 100 pA.

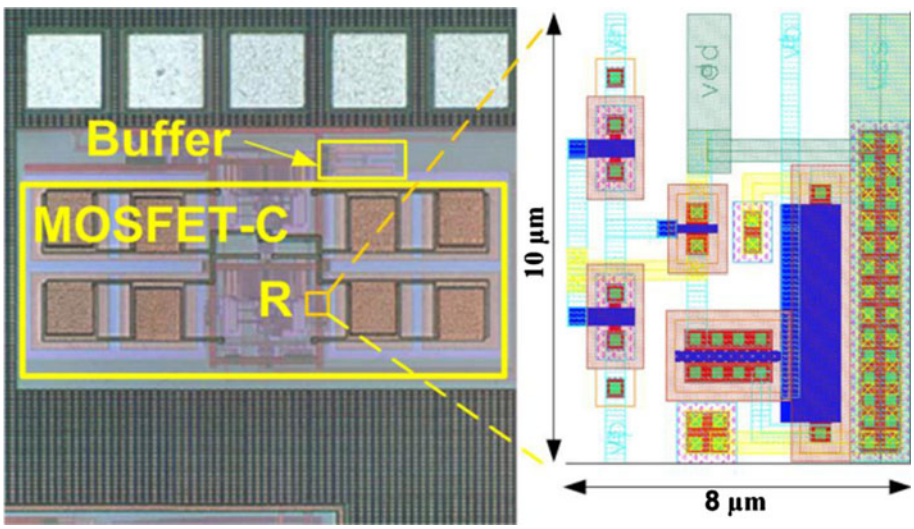

Fig. 10 Chip photomicrograph of the filter implemented with 0.18 μm CMOS technology (*inset*: implementation of the floating tunable resistors)

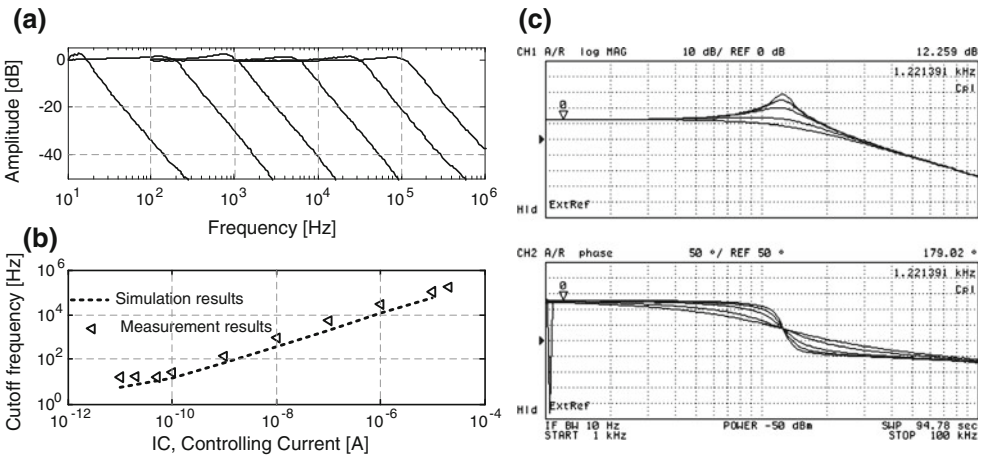

Fig. 11 Measured MOSFET-C filter characteristics: **a** frequency transfer characteristics. **b** cutoff frequency versus tuning current in comparison to the simulation results. **c** Q tuning by changing R2 value value at $I_C = 1$ nA

The normalized power consumption of the proposed second order filter is 1,080 pW/Hz.

Depicted in Fig. 11(c), it is possible to adjust the Q of the filter independent to the cutoff frequency through changing R2 in Fig. 9. Measured output phase of the proposed second order MOSFET-C filter shows that there is negligible variation on filter cutoff frequency when the quality factor of the filter is changing. On the other hand, based on Fig. 11(a) changing the cutoff frequency does not change the quality factor of the filter.

As shown in [18] and [19], an on-chip phase-locked loop (PLL) based tuning system will be employed in the final design to control the bandwidth of the filter. Figure 12 illustrated the tunability of the HVR based on experimental data. The tunability of the HVR corresponds to the tunability of the filter as shown in Fig. 11.

4.2 Dynamic range

Figure 13 shows the measured third harmonic distortion ($HD3 = H1/H3$) of the filter at different cutoff frequencies versus input signal amplitude. The cutoff frequency of the filter is adjusted with changing the controlling current as $I_C = 1$ nA to 10 μA. For each cutoff frequency, the input voltage swing is swept from −35 to 5 dBm. In each measurement, the frequency of the input signal has been selected to be four times smaller than the cutoff frequency of the filter. As can be seen, the linearity performance of the filter remains almost unchanged for the entire tuning range where the difference of the first and the third harmonics ($H1/H3$) are approximately 60 dB, and it can be maintained over four decades, for $A_{in} = -20$ dB (as the gain of filter is one, $A_{out} = -20$ dB).

The measured input referred third intercept point (IIP3) and noise of this filter are shown in Fig. 14(a)–(c). By changing the controlling current, I_C, the cutoff frequency has been changed, and in each point noise and IIP3 of the filter are measured. As expected, the total noise power remains fairly constant over the entire tuning range. The total integrated noise for this filter is in the range of

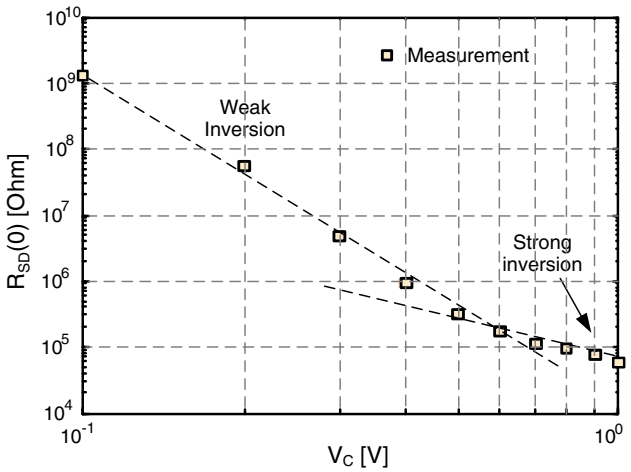

Fig. 12 Measured absolute value of the proposed floating resistance in different source-gate voltage values

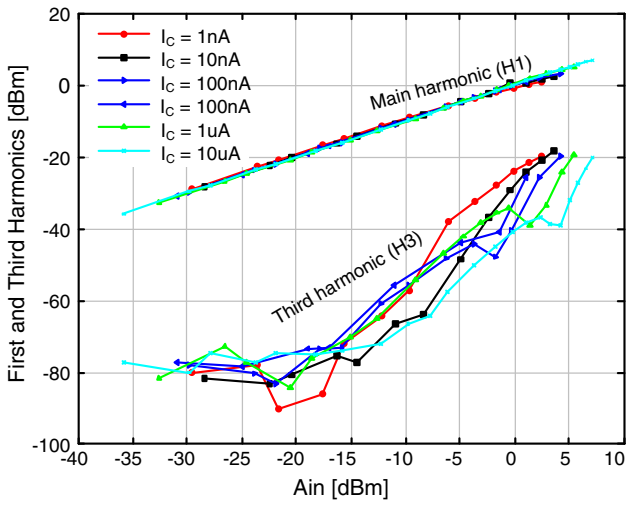

Fig. 13 Measured third harmonic for different cutoff frequencies. Cutoff frequency has been adjusted through controlling current, I_C. Here, the reference voltage is 50 Ω

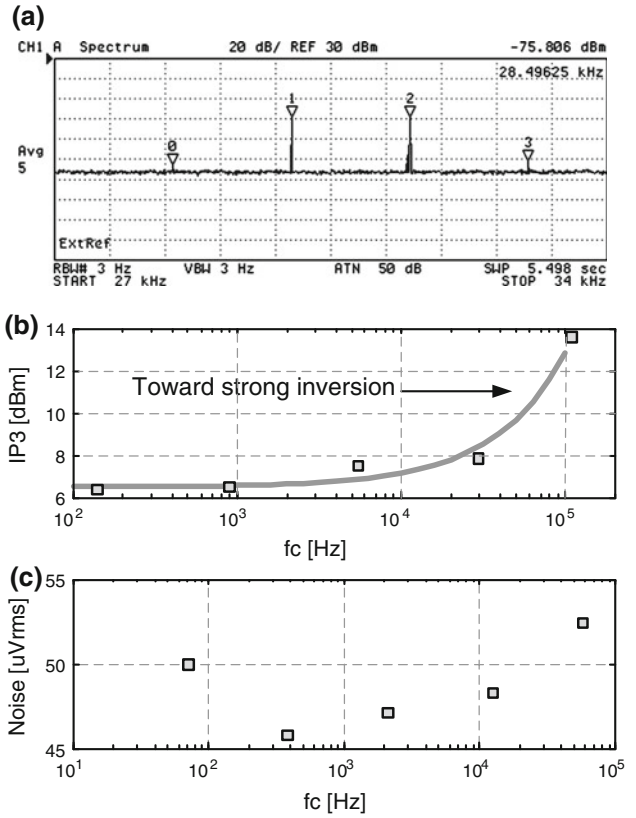

Fig. 14 Measured results: **a** spectrum of the output signal, **b** third order intermodulation intercept point, and **c** noise, of the proposed MOSFET-C filter. Here, the reference voltage is 50 Ω

45–55 μV_{rms} when the cutoff frequency is changing from about 80 Hz to 184 kHz.

Meanwhile, as long as the devices in the proposed floating resistors are in subthreshold regime, the filter exhibits a constant IIP3. When the devices enter into strong inversion, IIP3 improves by increasing the controlling current. This behavior can be seen in measurements as depicted in Fig. 14(b). The IIP3 of the filter is slightly less than 8 dBm for low cutoff frequencies and starts to increase for frequencies above 10 kHz and finally reaches to 14 dBm for $f_C = 100$ kHz.

4.3 Comparison and figure of merit

Table 1 summarizes the specifications of the filter. This filter consumes 540 pW/Hz/pole and occupies 0.045 mm^2/pole area. As the comparison in Table 1 shows, using high-valued resistors and avoiding less power efficient techniques such as transconductance scaling, or current division [1, 2, 20, 21] has resulted in much less normalized power dissipation. The figure of merit (FoM) that is achieved based on this definition [22]:

Table 1 Specifications of the proposed filter in comparison to some other works

Parameter	This work	[1]	[2]
V_{DD} (V)	1.8	±1.5	±1.5
Technology	0.18 µm	0.8 µm	0.8 µm
Order	2	6	1
$f_{c,min}$ (Hz)	20	2.4	0.016
$f_{c,Max}$ (Hz)	184 k		0.8
$f_{c,Max}/f_{c,min}$ (Hz/Hz)	9,200		50
Normalized P_{diss} (pW/Hz/pole)	540	694×10^3	287×10^3
Area (mm^2)	0.09	1	0.1
Normalized area (mm^2/pole)	0.045	0.17	0.1
Noise (μV_{rms})	50		50
IIP3 (dBm)	9		
IMFDR (dB)	70		
FOM	202		

$$FOM = 10\log\left(\frac{IMFDR_{lin.} \times \Gamma_f}{P_{diss}/(N \times f_c)}\right) \quad (11)$$

is 202. Here, $IMFDR_{lin.}$ stands for intermodulation free dynamic range, and Γ_f indicates the ratio of the maximum to minimum filter cutoff frequencies. Figure 15 compares the figure of merit of this filter with some other already published reports [22–39]. The improvement observed for this design is mainly due to the simple topologies that have been used to implement the circuits. This approach also results in a very area and power efficient filter. As the comparison in Table 1 shows, using high-valued resistors and avoiding less power efficient techniques such as transconductance scaling, or current division has resulted in much higher power efficiency.

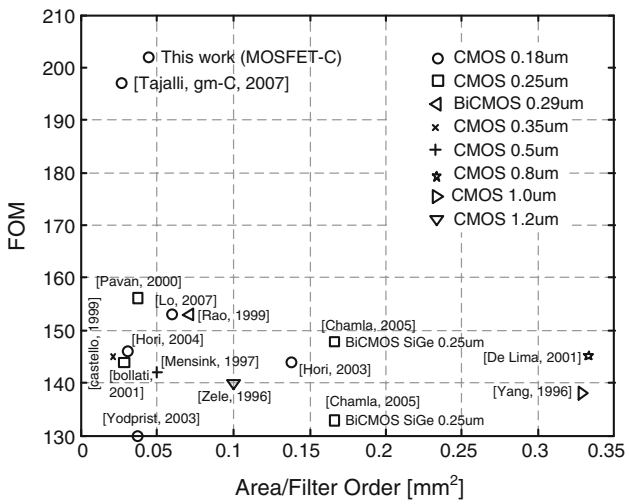

Fig. 15 FOM comparison to some other reports versus normalized filter area (area is normalized to the order of each filter). The data points used in this figure are extracted from [22–39]

5 Conclusions

Novel circuit techniques for implementing very high-valued and compact pseudoresistors ranging from few hundreds of MΩ to few hundreds of GΩ, have been introduced and analyzed. Using the proposed high-value resistance, a very low frequency and power-efficient MOSFET-C filter has been implemented. Consuming 540 pW/Hz/pole, the power dissipation of this filter changes linearly with the cutoff frequency of the filter which can be tuned over 20 Hz–184 kHz. Very low power dissipation, and small area occupation (0.045 mm^2/pole), as well as simple design process, make this filter very suitable for implantable, battery-less biomedical applications.

Acknowledgments The authors would like to thank S. Hauser for preparing the test setup. This work has been supported in part by the Nano-Tera research program (ULP-Logic) funded by the Swiss Confederation.

References

1. Solis-Bustos, S., Silva-Martinez, J., Molaberti, F., & Sanchez-Sinencio, E. (2000). A 60-dB dynamic-range CMOS sixth-order 2.4-Hz low-pass filter for medical applications. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 47*(12), 1391–1395.
2. Rieger, R., Demosthenous, A., & Taylor, J. (2004). A 230-nW 10-s time constant CMOS integrator for an adaptive nerve signal amplifier. *IEEE Journal of Solid-State Circuits, 39*(11), 1968–1975.
3. Harrison, R. R., & Charles, C. (2003). A low-power low-noise CMOS ampifier for neural recording applications. *IEEE Journal of Solid-State Circuits, 38*(6), 958–965.
4. Becker-Gomez, A., Cilingiroglu, U., & Silva-Martinez, J. (2003). Compact sub-Hz OTA-C filter design with interface-trap charge pump. *IEEE Journal of Solid-State Circuits, 38*(6), 929–934.
5. Majidzadeh, V., Schmid, A., & Leblebici, Y. (September, 2009). A fully on-chip LDO voltage redulator for remotely powered cortical implants. *European solid-state circuits conference (ESSCIRC)* (pp. 424–427).
6. Yin, M., & Ghovanloo, M. (May, 2007). A low-noise preamplifier with adjustable gain and bandwidth for biopotential recording applications. *IEEE international symposium on circuits and systems (ISCAS)* (pp. 27–30).
7. Tajalli, A., Leblebici, Y., & Brauer, E. J. (2008). Implementing ultra-high-value floating tunable CMOS resistors. *IEE Electronics Letters, 44*(5), 349–350.
8. Tajalli, A., & Leblebici, Y. (September, 2009). A widely-tunable and power-scalable MOSFET-C filter operating in subthreshold. In *Custom integrated circuits conference (CICC)* (pp. 593–596). San Jose, USA.
9. Papananos, Y., Georgantas, T., & Tsividis, Y. (1997). Design considerations and implementation of very low frequency continuous-time CMOS monolithic filters. *IEE Proceedings Circuits, Devices and Systems, 144*(2), 68–74.
10. Banu, M., & Tsividis, Y. (1983). Fully integrated active RC filters in MOS technology. *IEEE Journal of Solid-State Circuits, 18*(6), 644–651.
11. Zou, X., Xu, X., Yao, L., & Lian, Y. (2009). A 1-V 450-nW fully integrated programmable biomedical sensor interface chip. *IEEE Solid-State Circuits, 44*(4), 1067–1077.
12. Chae, M., Liu, W., Yang, Z., Chen, T., Kim, J., Sivaprakasam, M., & Yuce, M. (February 2008). A 128-channel 6mW wireless neural recording IC with on-the-fly spike sorting and UWB tansmitter. *IEEE international solid-state circuits conference (ISSCC)* (pp. 146–147).
13. Wattanapanitch, W. (2007). An energy-efficient micropower neural recording amplifier. *IEEE Transactions on Biomedical Circuits and Systems, 1*, 136–147.
14. Olsson, R. H., III, Buhl, D. L., Sirota, A. M., Buzsaki, G., & Wise, K. D. (2005). Band-tunable and multiplexed integrated circuits for simultaneous recording and simulation with microelectrode arrays. *IEEE Transactions on Biomedical Engineering, 52*(7), 1303–1311.
15. Tajalli, A., Vittoz, E., Leblebici, Y., & Brauer, E. J. (September, 2007). Ultra low power subthreshold MOS current mode logic circuits using a novel load device concept. In *Proceedings of European solid-state circuits conference (ESSCIRC)* (pp. 281–284). Munich, Germany.
16. Enz, C., Krummenacher, F., & Vittoz, E. (1995). An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. *Analog Integrated Circuits and Signal Processing Journal, 8*, 83–114.
17. Sansen, W. (2006). *Analog design essentials*. New York: Springer Publisher.
18. Tajalli, A., & Leblebici, Y. (September, 2010). A 9 pW/Hz adjustable clock generator with 3-decade tuning range for dynamic power management in subthreshold SCL systems. *European solid-state circuits conference (ESSCIRC)*.
19. Tajalli, A., & Leblebici, Y. (March, 2010). Ultra-low power mixed-signal design platform using subthreshold source-coupled circuits. *Design, Automation, & Test in Europe (DATE)*.
20. Veeravalli, A., Sanchez-Sinencio, E., & Silva-Marzinez, J. (2002). Transconductance amplifier structures with very small transconductances: A comparatice design approach. *IEEE Journal of Solid-State Circuits, 37*(6), 770–775.
21. Veeravalli, A., Sanchez-Sinencio, E., & Silva-Marzinez, J. (2002). A CMOS transconductance amplifier architecture with wide tuning range for very low frequency applications. *IEEE Journal of Solid-State Circuits, 37*(6), 776–781.
22. Chamla, D., Kaiser, A., Cathelin, A., & Belot, D. (2005). A $G_m - C$ low-pass filter for zero-IF mobile applications with a very wide tuning range. *IEEE Journal of Solid-State Circuits, 40*(7), 1143–1150.
23. Lo, T.-Y., & Hung, C.-C. (2007). A wide tuning range $G_m - C$ continuous-time analog filter. *IEEE Transactions on Circuits and Systems I, Fundamental Theory Applications, 54*(4), 713–722.
24. Tajalli, A., & Leblebici, Y. (2007). Wide tuning range linearity improved biquadratic transconductor-C filter. *IEE Electronics Letters, 43*(24), 1360–1362.
25. Stevenson, J.-M., et al. (February, 2007). A multi-standard analog and ddigital TV tuner for cable and terrestrial applications. In *Proceedings of IEEE international solid-state circuits conference (ISSCC) digest of technical papers* (pp. 210–211).
26. Fields, J., et al. (February, 1997). A 200 Mb/s CMOS EPRML channel with integrated servo demodulator for magnetic hard disks. In *Proceedings of IEEE international solid-state circuits conference (ISSCC) digest of technical papers* (pp. 314–315).
27. Bruschi, P., Sebastiabo, F., & Nizza, N. (2006). CMOS transconductors with nearly constant input ranges over wide tuning range. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 53*(10), 1002–1006.
28. Pavan, S., Tsividis, Y., & Nagaraj, K. (2000). Widely programmable high-frequency continuous-time filters in digital CMOS technology. *IEEE Journal of Solid-State Circuits, 35*(7), 503–511.

29. Bollati, G., Marchese, S., Dimecheli, M., & Castello, R. (2001). An eight-order CMOS low-pass filter with 30–120 MHz tuning range and programmable boost. *IEEE Journal of Solid-State Circuits, 36*(7), 1056–1066.
30. Banu, M., & Tsividis, Y. (1985). An elliptic continuous-time CMOS filter with on-chip automatic tuning. *IEEE Journal of Solid-State Circuits, 20*(6), 1114–1121.
31. Rao, N., Balan, V., & Contreras, R. (1999). A 3-V 10–100-MHz continuoustime seventh-order 0.05 equiripple linear phase filter. *IEEE Journal of Solid-State Circuits, 34*, 1676–1682.
32. De Lima J. A., & Dualibe, C. (2001). A linearly tunable low voltage CMOS transconductor with improved common-mode stability and its application togm-C filters. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 48*(7), 649–660.
33. Hori, S., Maeda, T., Matsuno, N., & Hida, H. (2004). Low-power widely tunable Gm-C filter with an adaptive dc-blocking, triode-biased MOSFET transconductor. In *Proceedings of European solid-state circuits conference (ESSCIRC)* (pp. 99–102). Leuven, Belgium.
34. Hori, S., Maeda, T., Yano, H., Matsuno, N., Numata, K., Yoshida, N., et al. (2003). A widely tunable CMOS Gm-C filter with a negative source degeneration resistor transconductor. In *Proceedings of European solid-state circuits conference (ESSCIRC)* (pp. 449–452). Estoril, Portugal.
35. Zele, R. H., & Allstot, D. J. (1996). Low-power CMOS continuous-time filters. *IEEE Journal of Solid-State Circuits, 31*(12), 157–168.
36. Mensink, C. H. J., Nauta, B., & Wallinga, H. (1997). A CMOS 'Soft-Switched' transconductor and its application in gain control and filters. *IEEE Journal of Solid-State Circuits, 32*(7), 989–998.
37. Castello, R., Bietti, I., & Svelto, F. (February, 1999). High-frequency analog filters in deep-submicron CMOS technology. In *IEEE international solid-state circuits conference (ISSCC) digest technical papers* (pp. 74–75).
38. Yodprasit, U., & Enz, C. (2003). A 1.5-V 75-dB dynamic range third-order $G_m - C$ filter integrated in a 0.18 μm standard digital CMOS process. *IEEE Journal of Solid-State Circuits, 38*(7), 1189–1197.
39. Yang, F., & Enz, C. (1996). A low-distortion BiCMOS seventh-order bessel filter operating at 2.5 V supply. *IEEE Journal of Solid-State Circuits, 31*(3), 321–330.

Armin Tajalli received the B.Sc. and M.Sc. degrees (Hons.) in Electrical Engineering from Sharif University of Technology, Tehran, and Tehran Polytechnic University in 1997 and 1999, respectively, and the Ph.D. degree from Swiss Federal Institute of Technology (EPFL) in 2010. From 1998 to 2006 he was with Emad Semicon as a Senior Analog Design Engineer. From 2010 he has been with Kandou Technologies developing architectures and circuits for very high-speed serial data transceivers. His research interests include broadband data communication circuits, wireless transceivers, phase-locked loops and synthesizers, A/D and D/A converters, and design of ultra-low power integrated circuits. He has received the Kharazmi Award on Research and Development, 2000, Outstanding Design Engineer, Emad Semicon, 2001, Presidential Award of the best Iranian researchers, 2003, AMD/CICC Student Award, 2009, and EPFL Prime Special Award, 2009. Dr. Tajalli is a coauthor of Extreme Low-Power Mixed Signal IC Design: Subthreshold Source-Coupled Circuits (Springer, 2010). He has served as a technical program committee member in IEEE International Conference on Computer Design (ICCD), 2010.

Yusuf Leblebici received his B.Sc. and M.Sc. degrees in Electrical Engineering from Istanbul Technical University, in 1984 and in 1986, respectively, and his Ph.D. degree in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign (UIUC) in 1990. Between 1991 and 2001, he worked as a faculty member at UIUC, at Istanbul Technical University, and at Worcester Polytechnic Institute (WPI). In 2000–2001, he also served as the Microelectronics Program Coordinator at Sabanci University. Since 2002, Dr. Leblebici has been a Chair Professor at the Swiss Federal Institute of Technology in Lausanne (EPFL), and director of Microelectronic Systems Laboratory. His research interests include design of high-speed CMOS digital and mixed-signal integrated circuits, computer-aided design of VLSI systems, intelligent sensor interfaces, modeling and simulation of semiconductor devices, and VLSI reliability analysis. He is the coauthor of 5 textbooks, namely, Hot-Carrier Reliability of MOS VLSI Circuits (Kluwer Academic Publishers, 1993), CMOS Digital Integrated Circuits: Analysis and Design (McGraw Hill, 1st Edition 1996, 2nd Edition 1998, 3rd Edition 2002), CMOS Multichannel Single-Chip Receivers for Multi-Gigabit Optical Data Communications (Springer, 2007), Fundamentals of High Frequency CMOS Analog Integrated Circuits (Cambridge University Press, 2009), and Extreme Low-Power Mixed Signal IC Design: Subthreshold Source-Coupled Circuits (Springer, 2010), as well as more than 200 articles published in various journals and conferences. He has served as an Associate Editor of IEEE Transactions on Circuits and Systems (II), and IEEE Transactions on Very Large Scale Integrated (VLSI) Systems. He has also served as the general co-chair of the 2006 European Solid-State Circuits Conference, and the 2006 European Solid State Device Research Conference (ESSCIRC/ESSDERC). He has been elected as Distinguished Lecturer of the IEEE Circuits and Systems Society for 2010–2011.