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MIXED SIGNAL LETTER

Low-voltage low-power Gm-C filters: a modified configuration for improving performance

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Abstract In this paper, after addressing the effect of finite output impedance of Gm cells on the performance of Gm-C filters, a modified configuration suitable for low-voltage operation is presented. In the proposed architecture, to efficiently increase the output impedance, body-driven impedance boosting is employed. The circuit-level topology of Gm cells is modified in order to increase the output impedance with minimized power consumption. To show the effectiveness of the proposed scheme, a 0.9-V 5-th order Butterworth low-pass filter with 8 MHz cutoff frequency is designed and simulated in 90-nm CMOS technology. Employing the proposed technique, power consumption is reduced from 0.7 mW to 0.5 mW.

Keywords Gm-C filter · Low voltage · Low power · Output impedance · Tansconductor

1 Introduction

Gm-C filters have been widely employed in high-frequency applications; with Gm-C integrators as the most important building blocks. In low-voltage CMOS technologies, several design challenges emerge some of which to be counted are limited output swing and reduced output impedance. As a result, modified Gm cell configurations applicable to low-voltage environments are getting increasingly popular [1–3].

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A low-voltage configuration for Gm cells is proposed and modified in this work. To this end, Sect. 2, discusses about the effects of transconductor finite output impedance on the performance of Gm-C filters. Our modified circuit for transconductors is later proposed in Sect. 3. This is followed by simulation results in Sect. 4 and conclusions in Sect. 5.

2 Effects of Gm cells finite output impedance on the performance of Gm-C filter

In Gm-C filters, transconductor-related non-ideal effects affecting the performance especially at higher frequencies, are finite output impedance, parasitic poles and zeroes and non-linearity. In highly-scaled CMOS technologies in which the supply voltage is small and where deep-sub-micron effects emerge, the output impedance of the transconductor is reduced and its linearity is degraded [3, 4]. The effect of finite output impedance of the transconductor on the performance of Gm-C filter is studied here in this section. To investigate the effect of output impedance on the performance of Gm-C filter, a 5-th order ladder filter, as shown in Fig. 1(a), is considered. Each floating inductor of this butterworth filter is substituted with four transconductors and one capacitor.

Figure 1(b) shows that the effect of finite output impedance of the transconductors is equivalent to a resistance in series with an inductor obtained from the following equation [5]

$$\frac{V_a - V_b}{i_i} = \frac{sC + 2G_o}{G_m^2} \equiv sL + R_s \Rightarrow L = \frac{C}{G_m^2} \;\&\; R_s = \frac{2G_o}{G_m^2} \tag{1}$$

where $G_o = 1/R_o$ models the output conductance of each non-ideal transconductor.

This equation shows that decreasing the output impedance of the transconductor is equivalent to an increased

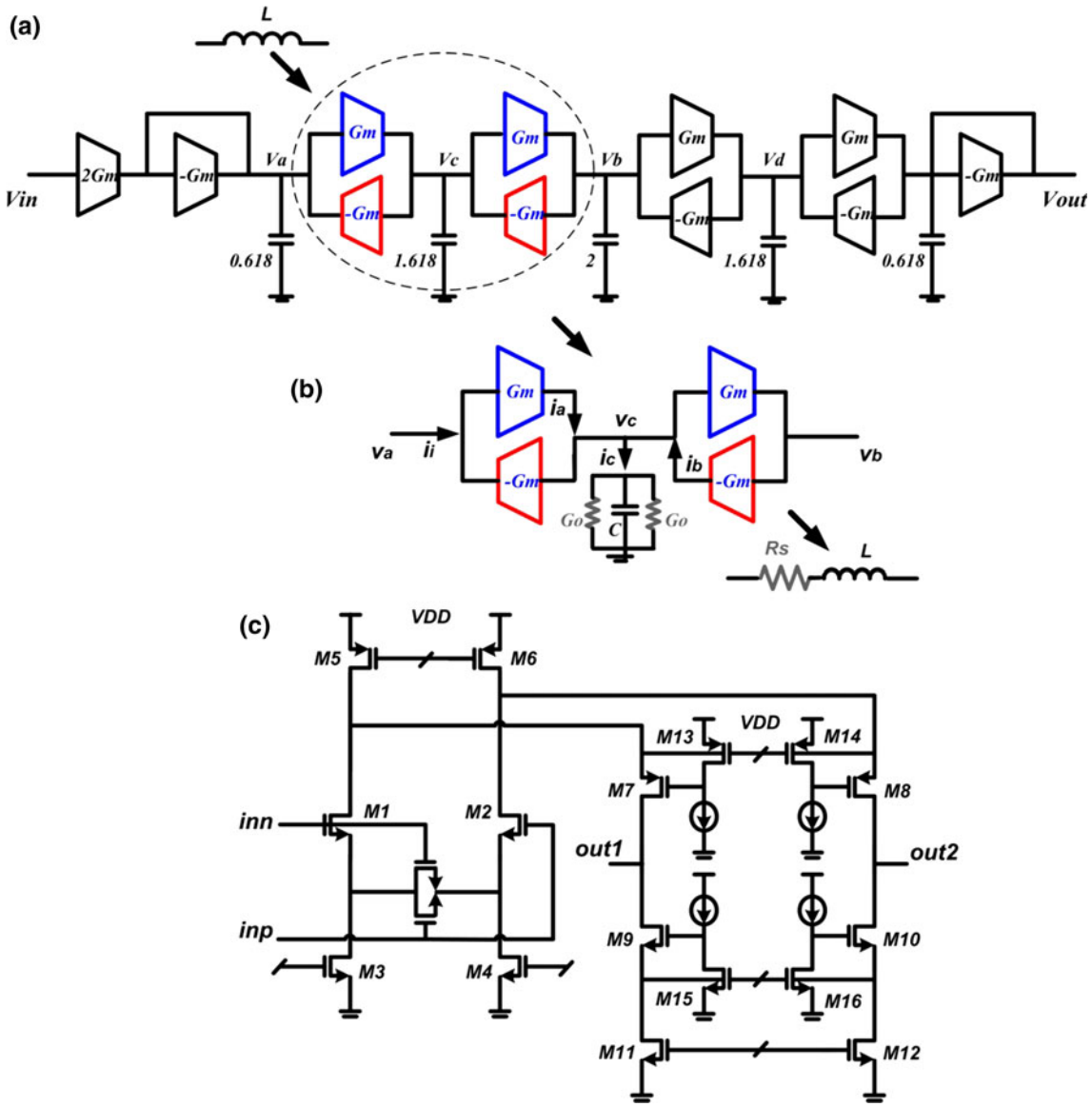

Fig. 1 **a** Block diagram of a 5-th order butterworth filter, **b** Implementation of the floating inductor with the effect of finite output impedance of transconductors included, **c** Schematic of the body-driven impedance-boosted folded-cascode transconductor

series resistance of the inductor. The DC gain of the filter is thus reduced.

Non-idealities of transconductors are usually evaluated by means of excess phase shift at the unity gain frequency. As a result, the phase error of the integrator in unity gain frequency changes the specifications of the filter [3]. The transfer function of the ideal integrator is given by

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_m}{sC} \tag{2}$$

where Gm is DC transconductance.

Considering the non-idealities of the transconductor, the transfer function of Gm-C integrators can be written as

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_m\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_p}\right)}\frac{1}{sC+G_o} \tag{3}$$

where ω_p *and* ω_z are the parasitic pole and zero, respectively. To calculate the phase value at the unity-gain frequency $\omega_o = {}^{G_m}/_{C}$, one can write

$$\begin{aligned}\Rightarrow arg[H(j\omega)] &\approx \tan^{-1}\frac{\omega_o}{\omega_z} - \tan^{-1}\frac{\omega_o}{\omega_p} - \tan^{-1}\frac{G_o}{\omega_o C}\\ &= \tan^{-1}\frac{\omega_o}{\omega_z} - \tan^{-1}\frac{\omega_o}{\omega_p} - \left(\frac{\pi}{2} - \tan^{-1}\frac{G_o}{G_m}\right)\end{aligned}$$

$$if\ G_mR_o \gg 1, \omega_z, \omega_p \gg \omega_o \Rightarrow arg[H(j\omega)] \approx \frac{\omega_o}{\omega_z} - \frac{\omega_o}{\omega_p} - \frac{\pi}{2} + \frac{1}{G_mR_o} \quad (4)$$

Based on Eq. 4, the phase error (θ_p) at unity-gain frequency is obtained from

$$\theta_p \approx \frac{1}{G_mR_o} + \omega_o\left(\frac{1}{\omega_z} - \frac{1}{\omega_p}\right) \quad (5)$$

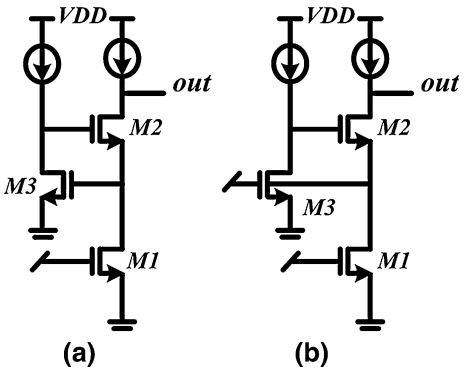

Fig. 2 **a** Gate-driven gain-boosted cascode amplifier, **b** body-driven gain-boosted cascode amplifier

Eq. 5 highlights a very important role of the output impedance. It shows that increasing the output impedance decreases the phase error.

3 Proposed circuit for the transconductor

As explained earlier, finite output impedance of the transconductor degrades the performance of the Gm-C filter. Different techniques can be used to increase the output impedance of the transconductor [6, 7]. However, they are not suitable for low-voltage and high-frequency applications.

Figure 1(c) shows the proposed transconductor circuit which is based on folded-cascode configuration. In this circuit, in order to efficiently increase the output impedance, body-driven impedance boosting has been employed. Furthermore, source degeneration has been used for input devices to improve linearity [8]. The main advantage of this linearization technique is its application for low-voltage circuits.

The effectiveness of the proposed technique for the transconductor output stage over the basic gain-boosted cascode amplifier (as shown in Fig. 2(a)) can be understood from Fig. 2(b). In Fig. 2(a), the drain-source voltage of M_1 is stabilized by V_{GS} of the gain boosting device, M_3.

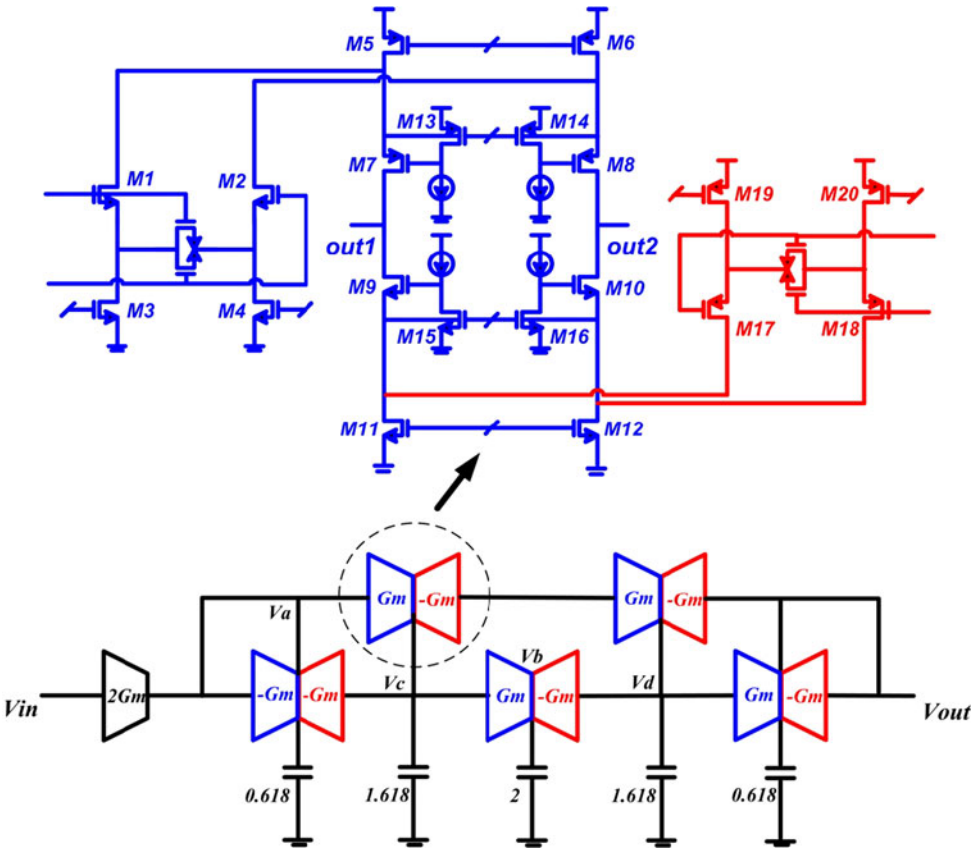

Fig. 3 The modified architecture of the Gm-C filter

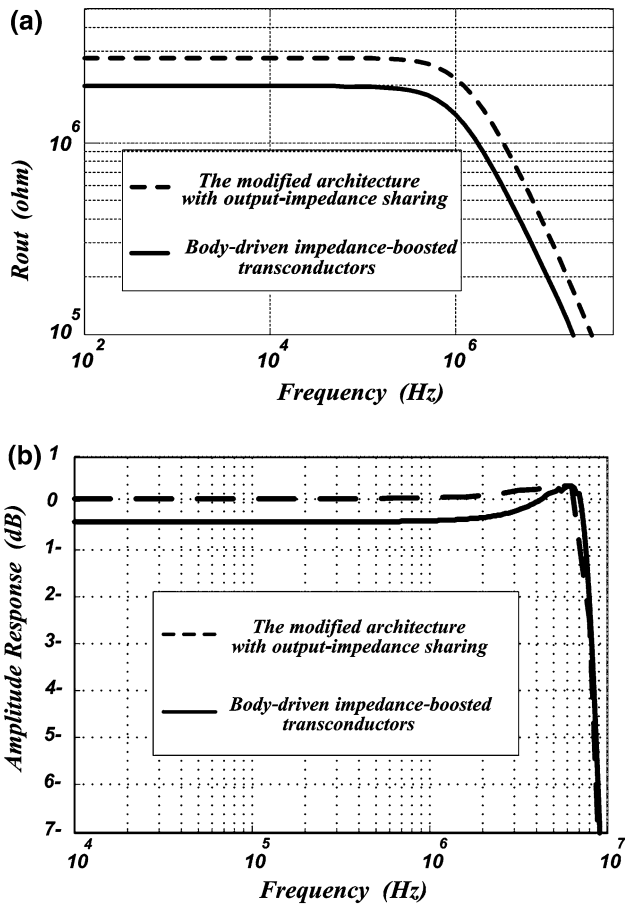

Fig. 4 Comparison between simulation results of the two architecture. **a** Improvement of output impedance, **b** improvement of DC gain of the filter

The output resistance thus is enhanced. Notating V_{ov2}, V_{th2}, V_{ov3} and V_{th3} as the overdrive and threshold voltages of M_2 and M_3 respectively, the minimum value for the output voltage of this configuration thus is [9]

$$V_{out} = V_{GS3} + V_{ov2} = V_{th3} + V_{ov3} + V_{ov2} \tag{6}$$

which is usually large and unacceptable for low-voltage applications.

In Fig. 2(b), on the other hand, body-driven gain boosting is employed around a gate-driven cascode amplifier. Since the body-source voltage of M_3 imposes no limitation on minimum drain-source voltage of M_1, it can be biased on its minimum value of (V_{ov1}). The minimum value for the output voltage is consequently

$$V_{out} = V_{ov1} + V_{ov2} \tag{7}$$

As a result, the output voltage swing is increased and the minimum voltage of the power supply can be reduced. The transconductor described in Fig. 1(c), is used in ladder filter of Fig. 1(a).

To alleviate the degrading effect of reduced output impedance of transconductors connected to the same capacitors (where the output impedances are paralleled), the block diagram of the filter is modified as shown in Fig. 3. In this modified architecture, two transconductors with common outputs are combined in a way that the input stages are different but the output stage is shared. In this way, as compared with Fig. 1, not only the output impedance of transconductors is enhanced, but also power and area is saved.

From now on, we are going to demonstrate the improvement of output impedance with analytical derivations. At first, the output impedance of the transconductor of Fig. 1(c), is [7]

$$Rout_1 \approx A_{v15} g_{m9} r_{O9} r_{O11} || A_{v13} g_{m7} r_{O7} (r_{O5} || r_{O1})$$

$$A_{v15} \approx g_{mb_{15}} r_{O15} \;\&\; A_{v13} \approx g_{mb_{13}} r_{O13}$$

where $g_{mb_{15}}$ & $g_{mb_{13}}$ are the body transconductance of M_{15} and M_{13}.

Using the following approximations:

$$A_{v15} \approx A_{v13} = A_v \;\&\; g_{m9} \approx g_{m7} = g_m$$

$$r_{O11} \approx r_{O1} = r_O \;\&\; r_{O5} \approx \frac{r_O}{2}$$

The output resistance is thus estimated as

$$\Rightarrow Rout_1 \approx A_v g_m r_O^2 || A_v g_m r_O \left(\frac{r_O}{2} || r_O\right) = A_v g_m r_O^2 || A_v g_m \frac{r_O^2}{3} = A_v g_m \frac{r_O^2}{4}$$

The weak point of Fig. 1(a) is that the output impedance of two transconductor are paralleled. Thus, the output impedance at the node V_C of the filter becomes

$$Rout_1 \approx A_v g_m \frac{r_O^2}{4} || A_v g_m \frac{r_O^2}{4} = A_v g_m \frac{r_O^2}{8} \tag{8}$$

Now, consider Fig. 3 as the proposed architecture. In this circuit the output impedance of node V_C is expressed as

$$Rout_1 \approx A_{v15} g_{m9} r_{O9} (r_{O11} || r_{O17}) || A_{v13} g_{m7} r_{O7} (r_{O5} || r_{O1})$$

Based on the following estimations

$$A_{v15} \approx A_{v13} = A_v \;\&\; g_{m9} \approx g_{m7} = g_m \;\&\; r_{O1} \approx r_{O17} = r_O \;\&\; r_{O5} \approx r_{O11} = \frac{r_O}{2}$$

The output resistance becomes

$$\Rightarrow Rout_1 \approx \left[A_v g_m r_O \left(\frac{r_O}{2} || r_O\right)\right] || \left[A_v g_m r_O \left(\frac{r_O}{2} || r_O\right)\right] = A_v g_m \frac{r_O^2}{3} || A_v g_m \frac{r_O^2}{3} = A_v g_m \frac{r_O^2}{6} \tag{9}$$

Comparing Eq. 8 with Eq. 9, the output impedance is improved by a factor of 8/6 for the modified architecture of Gm-C filter.

Table 1 Simulation results of 5-th order butterworth Gm-C filter

Transcondutors	Body-driven impedance boosting	Body-driven impedance boosting with output-impedance sharing
CMOS technology	90 nm	90 nm
Power supply	0.9 V	0.9 V
Cutoff frequency	8 MHz	8 MHz
DC gain of the filter	0.955	0.994
Output impedance(Rout) @ e. g. Vc	1975 k	2775 k
Power consumption	0.7 mW	0.5 mW
THD @ $0.4V_{PP}$	1.1 %	0.7 %

4 Simulation results

The proposed transconductor is employed to design a 5-th order Butterworth low-pass Gm-C filter. Simulation results of the filter in a 90-nm CMOS technology show that power consumption is reduced when body-driven impedance-boosted transconductors of Fig. 1 is substituted with output-impedance sharing architecture of Fig. 3 (0.7 mW vs. 0.5 mW). DC gain of the filter, as illustrated in Fig. 4(b), increases from −0.4 to −0.05 dB after employing the modified technique.

Table 1 compares the performance of the two architecture of 5-th order butterworth Gm-C filters. Simulation results are presented in Fig. 4 .

5 Conclusion

A CMOS implementation of a 5-th order Butterworth low-pass Gm-C filter was presented. An impedance-enhancement technique has been employed for Gm cells to overcome the output-impedance reduction phenomenon that is common in low-voltage deep-sub-micron applications. The new method has shown that the influence of low output impedance can be interpreted as a droop in passband. The results also shows that the excess phase will produce distortion in transfer function and 0.31 dB peak in output voltage. Simulation results of the Gm-C filter with shared output stages of the transconductors confirm the effectiveness of the proposed method in reducing the power consumption while filter performance is improved.

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