A Widely-Tunable and Ultra-Low-Power MOSFET-C Filter Operating in Subthreshold

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***Abstract*— A very wide tuning range ultra-low-power MOSFET-C filter is presented. The wide tuning range in this filter has been achieved without using any switchable components or programmable building blocks, and the cutoff frequency of the filter can be adjusted simply through a controlling bias current. The filter has low-pass characteristics with f_c = 20Hz to 184kHz while exhibiting a constant power consumption per cutoff frequency over its entire tuning range that is almost four decades wide. The proposed MOSFET-C filter uses PMOS transistors in subthreshold regime for implementing floating and widely adjustable resistors. The ultra high resistivity of the PMOS devices makes them very suitable for implementing very low frequency and compact filters. Realized in 0.18μm CMOS technology, the filter exhibits a relatively constant noise and linearity performance over its entire tuning range. The active area of the proposed MOSFET-C filter is 0.09mm^2.**

I. Introduction

Emerging new markets for multi-purpose and multi-standard applications increase the importance and significance of designing reconfigurable integrated circuits (ICs) [1], [2]. Having wide tuning frequency range is one of the most important aspects needed in design of reconfigurable circuits. To achieve a power efficient and widely tunable integrated circuit, it is desirable to have proportional power consumption (P_{diss}) and frequency of operation (f_{op}), i.e.: $P_{diss} \propto f_{op}$. While digital CMOS integrated circuits can inherently cover a very wide range of operating frequencies with scalable power consumption [3], in analog integrated circuits it is generally very difficult to have these properties simultaneously.

Changing the biasing condition to change the operating frequency of an analog circuit has generally complex effects on the circuit performance, specially on circuit dynamic range (DR). Therefore, this approach is only useful for few tens of percent variation of the desired parameter over the nominal working condition. This is mainly because devices leave their intended regime of operation by changing the biasing condition. Some circuit techniques for extending the tuning range by changing the biasing condition of devices, especially MOS devices biased in triode region, are reported [4]. Bipolar devices or MOS transistors that biased in subthreshold regime and exhibit exponential I-V characteristics [5] can be employed to extend the range that circuit can be operated with changing the biasing conditions. A good example is log-domain integrated continuous-time filters (CTFs) that exhibit a very wide tuning range [6]. The other solution for extending the operating frequency range in analog integrated circuits is using some switchable or programmable components and building blocks [7]-[10]. The main issues associated with this approach are increasing the power consumption and silicon area as well as the circuit complexity. Meanwhile, by switching the devices or blocks, it is very difficult to control some of the main circuit parameters such as linearity and noise.

In this article, we introduce a new approach for implementing very low power and widely tunable MOSFET-C filter without using any switching components or building blocks. Based on this approach, subthreshold MOS devices have been used to implement very high-valued and floating resistors. As will be shown later, this topology is also very suitable for implementing very low frequency CTFs.

II. Widely Tunable MOSFET-C Filter

The cutoff frequency of a MOSFET-C filter can be adjusted by changing the size of capacitances or resistances. Using triode MOS based resistors, it is possible to have enough flexibility to compensate for the process and environmental variations and tune the filter cutoff frequency on the desired value [11]. There are also some reports using varactors to provide the desired tuning range [12]. However, to have a very wide tuning range, generally programmable capacitor or resistor banks are needed. The complexity and extra area due to the switchable components reduces the power and area efficiency of this approach.

A. Proposed Topology

Figure 1 proposes a first order MOSFET-C filter that uses a variable resistance for adjusting its cutoff frequency. Here, a widely tunable resistance and a high-gain and robust OTA with scalable power consumption are the main building blocks to implement a wide tuning range MOSFET-C filter. To scale the circuit power consumption with respect to the filter cutoff frequency (f_c), it is necessary to change the power consumption of the amplifier (through $I_{B,OP}$) proportional to f_c (or inversely proportional to R).

To have very wide tuning range as well as low power consumption, MOS devices biased in subthreshold regime can be utilized. The exponential I-V characteristics of MOS devices in subthreshold makes the wide variation of biasing condition possible. However, MOS devices in subthreshold regime have very poor linearity performance. Biased in subthreshold, a

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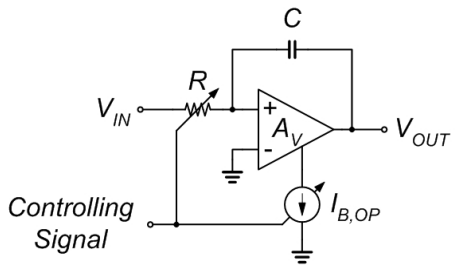

Fig. 1. Tunable active-RC (MOSFET-C) filter using variable resistor. The power consumption of the amplifier is scalable with respect to the filter cutoff frequency.

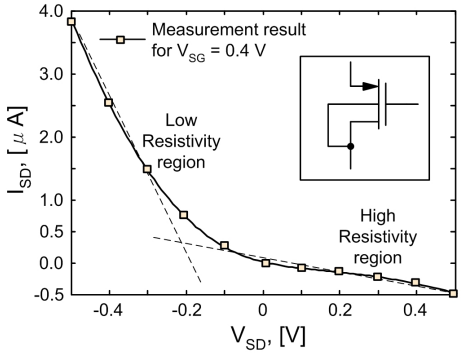

Fig. 2. Resistance implementation based on subthreshold PMOS device: proposed PMOS device (inset) and the measured I-V characteristics of the proposed floating resistor for $V_{SD} <_{\cdot} 0$V and $V_{SD} > 0$V

MOS device exhibits a medium linearity for voltage swing of only few $U_T = k \cdot T/q$ (q is the unit charge value, and k is the Boltzmann's constant). To extend the linearity range of the device without the need for very large size devices, the configuration of Fig. 2 (inset) can be utilized [13]. In this configuration, the bulk terminal of the PMOS device is connected to its drain, hence based on EKV model [5], [14]:

$$I_{SD} = I_0 \cdot e^{\frac{V_{DG}-V_{T0}}{n_p U_T}}(e^{\frac{V_{SD}}{U_T}} - 1) \quad (1)$$

in which $I_0 = 2n_p\mu C_{ox} \cdot \frac{W}{L_{eff}} U_T^2$ (n_p and μ are subthreshold slope factor and carrier mobility in PMOS device, respectively). Therefore, the equivalent resistance of this device is:

$$R_{SD} = (\frac{\partial I_{SD}}{\partial V_{SD}})^{-1} = (\frac{n_p U_T}{I_{SD}}) \cdot (\frac{e^{V_{SD}/U_T} - 1}{(n_p - 1)e^{V_{SD}/U_T} + 1}). \quad (2)$$

Based on (1), this device can be used as a resistor with medium linearity in a wider voltage swing compared to the conventional configuration biased in weak-inversion. The maximum voltage swing in this configuration is limited to about 500mV, where the source-bulk diode starts to conduct a current comparable to the drain current of this device.

Note that when V_{SD} becomes negative, the current direction is reversed and the device switches to conventional configuration in which the bulk is connected to source. In this case, the drain current will increase rapidly. This property can help to implement high valued *floating resistors* with a very wide adjusting range by connecting two PMOS transistors back-to-back as shown in Fig. 3(a). In this circuit, MP1 and MP2 are implementing high valued resistances and MN provides the necessary source-gate voltage for MP1 and MP2. The resistivity of this floating resistance can be adjusted by changing the source-gate voltage of PMOS devices through adjusting the bias current of MN (I_C). The measured I-V characteristics of this floating resistance show moderate linearity in a very wide voltage range. Based on measurement results shown in Fig. 3(b), this floating resistance exhibits medium linearity performance and has been used in this work to implement a widely tunable MOSFET-C filter. The adjustability range of the proposed floating resistance is shown in Fig. 3(c).

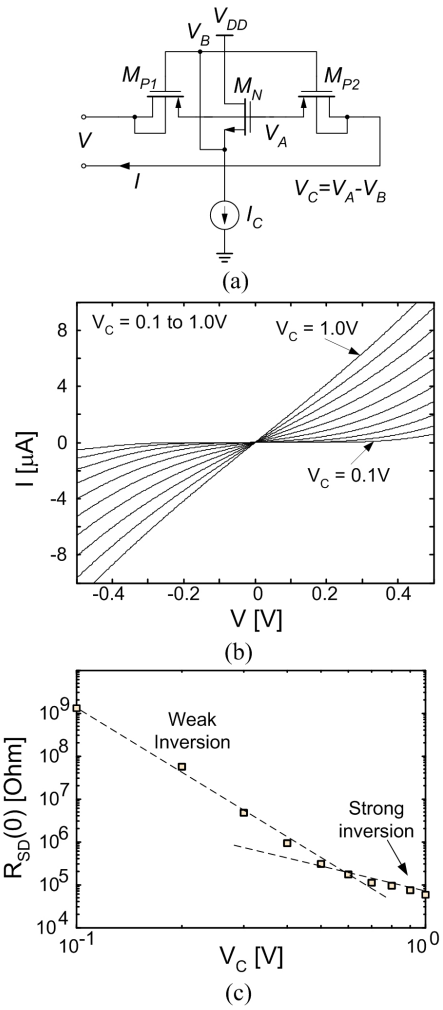

Fig. 3. Proposed floating resistance: (a) circuit schematic, (b) measured I-V characteristics of the proposed configuration for different V_C values, (c) measured resistance of the proposed floating resistor with respect to the gate-source voltage of MN ($V_C = V_{GS,MN} = V_{SG,MP1,2}$).

B. Dynamic Range

The topology of the MOSFET-C shown in Fig. 1 is well suited for implementing constant dynamic range (DR) widely adjustable filters. This property is mainly due to the almost constant *noise* and *linearity* performance of the filter while the cutoff frequency of the filter changes. The total rms (root-mean square) input referred noise of the filter shown in Fig. 1 is:

$$v_{n,rms,in}^2 = \gamma_F \cdot (k \cdot T/C) \tag{3}$$

in which γ_F indicates the circuit excess noise factor and depends on topology of the amplifier, resistances, and filter frequency transfer function especially filter quality factor (Q), k is Boltzmann's constant, and T is the junction temperature in kelvin. Regarding (3) and assuming that the noise of amplifier scales with its power consumption (or equivalently, assuming γ_F is bias independent), constant capacitor size results in constant rms filter noise in different cutoff frequencies.

On the other hand, based on (2) the linearity of the resistance introduced in Fig. 2 is independent to the bias current or V_{SG} and the dependence on V_{SD} is the same for different bias currents. Hence, as long as the devices are in subthreshold regime, the linearity performance of the resistance remains unchanged. The linearity improves by entering into the medium and strong inversion regions.

C. Amplifier

To implement a filter with scalable power consumption proportional to its cutoff frequency, it is necessary to design a scalable power amplifier. In this work a two stage amplifier topology has been utilized in which the unity gain-bandwidth (UGBW) of the amplifier is:

$$UGBW \simeq g_{m1}/(2\pi C_C) \tag{4}$$

which is proportional to g_{m1} (transconductance of the input stage), and inversely proportional to the compensation capacitance (C_C). Assuming the input devices are in subthreshold, then:

$$UGBW \simeq \frac{I_{SS}}{2nU_T} \cdot \frac{1}{2\pi C_C} \tag{5}$$

which is proportional to the bias current of the input stage of amplifier (I_{SS}). Meanwhile, to have a phase margin of at least 60° [16]:

$$f_{p,nd} \geq 3 \times UGBW \tag{6}$$

where, $f_{p,nd}$ is the non-dominant pole of the amplifier. Since the value of $f_{p,nd}$ is inversely proportional to the load resistance $G_L = 1/R_L$ (R_L is equivalent load resistance of the amplifier and is calculated in (2)) and G_L is proportional to the bias current, by proper choosing the size of devices, it is possible to make the inequality presented in (6) independent of bias current. Therefore, as long as the devices are in subthreshold regime, the stability of the circuit is guaranteed.

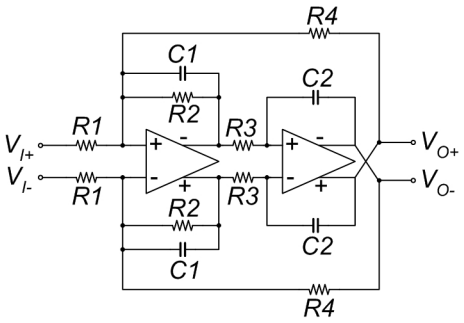

Fig. 4. A second order MOSFET-C filter. All the resistors are implemented using the floating resistor introduced in Fig. 3(a).

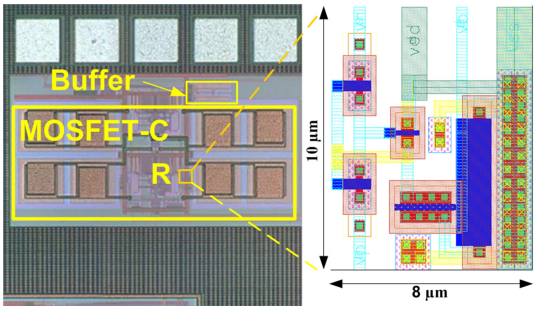

Fig. 5. Chip photomicrograph of the proposed filters implemented with 0.18μm CMOS technology.

III. Experimental Results

A second order MOSFET-C filter based on the topology shown in Fig. 4 has been implemented in 0.18μm CMOS technology. The chip photomicrograph of the filter is shown in Fig. 5. The proposed filter occupies a Si area of 420μm $\times$ 210μm while using MiM capacitors. As seen in Fig. 5, it is possible to compare the area of the proposed floating resistances with the size of other components in the circuit.

The measured frequency response of the filter versus input frequency controlling current (I_F) is shown in Fig. 6(a). In this measurement, the bias current of all resistors as well as the bias current of the amplifiers are scaled with respect to the I_F. As can be seen in this figure, the controlling current can be as low as I_C=100pA for $f_C \simeq$20Hz while the capacitors used to implement this filter are 2pF. Therefore, this topology can be also very suitable for implementing very low frequency filters. The normalized power consumption of the proposed second order filter is 1080pW/Hz. Figure 6(b) compares the tunability of this filter in comparison to the simulation results. As shown in Fig. 6(c), it is possible to adjust the Q of the filter independent to the cutoff frequency through adjusting R2 in Fig. 4.

The measured total rms noise and third intercept point (IP3) of this filter are about 50μV_{rms} and 9dBm, respectively. As expected, the noise level remains relatively constant for different cutoff frequencies. Meanwhile, as long as the devices in the

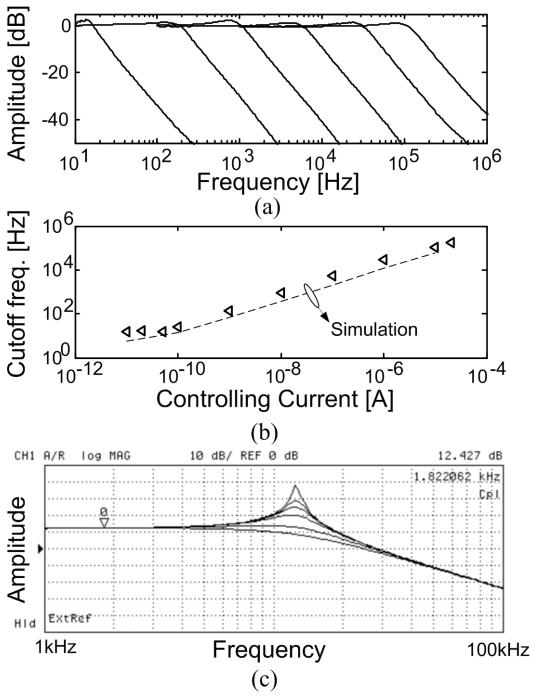

Fig. 6. Measured MOSFET-C filter characteristics: (a) frequency transfer characteristics, (b) cutoff frequency versus tuning current in comparison to the simulation results, (c) Q tuning by changing R2 value (I_C=1nA).

TABLE I

SPECIFICATIONS OF THE FILTERS

Parameter	MOSFET-C	Unit
V_{DD}	1.8	[V]
Technology	0.18μm CMOS	[-]
Order	2	[-]
$f_{c,min}$	20	[Hz]
$f_{c,Max}$	184k	[Hz]
$f_{c,Max}/f_{c,min}$	9'200	[Hz/Hz]
Normalized P_{diss}	540	[pW/Hz/pole]
Area	0.09	[mm^2]
Normalized Area	0.045	[mm^2/pole]
Noise	50	[μV$_{rms}$]
IP3	9	[dBm]
IMFDR	70	[dB]
FOM	202	[-]

floating resistors shown in Fig. 3(a) are in subthreshold regime, the filter exhibits a constant IP3. When the devices enter strong inversion, IP3 improves by increasing the controlling current.

Table I summarizes the specifications of the filter. This filter filter consumes 540pW/Hz/pole and occupies 0.045mm^2/pole area. The figure of merit (FoM) that is achieved based on definition in [15] is 202 which is much better compared to the other already published reports. This improvement is mainly due to the simple topologies used to implement the circuits which has also concluded in a very area efficient implementation.

IV. CONCLUSION

In this article, we introduce a continuous-time MOSFET-C filter with very wide tuning range and ultra-low power consumption. The proposed filter uses a compact floating resistor implemented by subthreshold PMOS devices that can be adjusted in a very wide range. This technique is especially suitable for implementing very low frequency filters with a good linearity and dynamic range. The filter uses constant capacitors which implies constant rms noise level for the entire tuning range. Measurements show that the linearity remains also almost constant for the entire tuning range that is four decades wide. The power consumption scales proportional to the cutoff frequency which makes this topology very power efficient, with figure of merit (FoM) of 202. Implemented in 0.18μm CMOS technology, the area of the proposed second order MOSFET-C filter is 0.09mm^2.

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