INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. (2014)
Published online in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.1985

A 0.8-V supply bulk-driven operational transconductance amplifier and Gm-C filter in 0.18 μm CMOS process

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SUMMARY

A low voltage bulk-driven operational transconductance amplifier (OTA) and its application to implement a tunable Gm-C filter are presented. The linearity of the proposed OTA is achieved by nonlinear terms cancelation technique, using two paralleled differential topologies with opposite signs in the third-order harmonic distortion term of the differential output current. The proposed OTA uses 0.8 V supply voltage and consumes 31.2 μW. The proposed OTA shows a total harmonic distortion of better than −40 dB over the tuning range of the transconductance, by applying 800 mV_{ppd} sine wave input signal with 1 MHz frequency. The OTA has been used to implement a third-order low-pass Gm-C filter, which can be used for wireless sensor network applications. The filter can operate as the channel select filter and variable gain amplifier, simultaneously. The gain of the filter can be tuned from −1 to 23 dB, which results in power consumptions of 187.2 to 450.6 μW, respectively. The proposed OTA and filter have been simulated in a 0.18 μm CMOS technology. Simulations of process corners and temperature variations are also included in the paper. Copyright © 2014 John Wiley & Sons, Ltd.

Received 7 October 2013; Revised 3 February 2014; Accepted 9 February 2014

KEY WORDS: OTA; low voltage; low power; bulk driven; Gm-C filter; wireless sensor networks

1. INTRODUCTION

Nowadays, low voltage, low power analog circuits play an important role in many applications such as wireless sensor networks (WSNs), to reduce their weight and increase their battery life time. In fact, the demand for analog circuits that operate with a low supply voltage has increased by these battery-powered applications. In WSNs, sometimes the nodes cannot be easily accessed, so they should operate few months or years on a single battery. Over time, the voltage of the battery drops. Therefore, the circuits in the nodes should be designed to operate with low supply voltages. On the other hand, having a high threshold voltage with respect to the decreasing supply voltage generates many issues in the design of these low voltage circuits.

A low voltage operational transconductance amplifier (OTA) is the main building block of many analog circuits such as filters, which are used in WSNs and other low voltage applications. The function of the OTA can be modeled as a voltage-controlled current source, which converts input voltage to output current. Because of its bias-based tunability and fast speed compared with the conventional opamps, it is a good choice for many applications. However, this cell has an important drawback. It has a very small input voltage range that yield 1% total harmonic distortion (THD) [1].

Many linearity improvement techniques have been reported in recent years, such as attenuation [2], source degeneration [3–5], nonlinear terms cancelation [6–11], and triode-based transconductor [12–14]. The linearity can be improved by adding resistance in source of the input transistors in the source

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degeneration technique. The noise factor of the source-degenerated OTA is larger in tradeoff with the improved linearity. Because source degeneration technique uses resistance in sources of the input transistors and the sources must not be grounded, this technique could be applied only to the fully differential architectures and could not be used for pseudo-differential ones. So, it is hard to reduce supply voltage in this technique because of more stacked transistors. Unlike this, nonlinear terms cancelation technique is more suitable for low supply voltage design, because in this technique, using pseudo-differential architecture for reducing the supply voltage is easier. In fact, in this technique, linearity improvement is achieved by means of an appropriate sum of the nonlinear terms to force the result to zero. Triode-based transconductor is another method that could be applied to pseudo-differential architectures. In this technique, drain-source voltage of triode transistors is kept constant, and this leads to a linear OTA with constant transconductance. In this technique, tuning of the transconductance value is achieved by varying the drain-source voltage of the triode transistors. These linearity improvement techniques are getting harder to achieve in low supply voltages. So, novel analog circuit design methods should be considered for low voltage operation.

Using bulk-driven transistors [15, 16], flipped voltage follower cell [17], pseudo-differential pairs [18], floating gate approach, sub-threshold MOSFET [16], and level shifter are some design methods reported for reduced supply voltage analog circuits. Although these techniques ruin most of the OTAs characteristics, such as noise, linearity, open loop DC gain, unity gain bandwidth, and common mode rejection ratio, merging these methods is necessary for ultra low voltage designs. For example, in [16], bulk-driven transistors are used in sub-threshold region for ultra low voltage design. Hence, a suitable topology and appropriate bias circuits should be used for getting optimized circuits.

In this work, a low voltage, low power, and linear transconductance amplifier is presented. The proposed OTA can work under a 0.8 V supply voltage in a 0.18 μm CMOS process for some related applications, such as WSNs. The linearity of the proposed OTA is achieved by nonlinear terms cancelation technique, using two paralleled differential topologies with opposite signs in the third-order harmonic distortion term of the differential output current. Because of the appropriate chosen circuit topology, the power consumption of the proposed circuit is achieved much lower than that of the OTA in [6], which used same linearity improvement technique but for gate driven structure. Transconductance enhancement technique [19] is applied to the circuit, in order to overcome some drawbacks of using bulk-driven structures, such as high noise, low bandwidth, and low DC gain. In [19], the technique is applied to a differential transconductor, while in this work, we have applied it to a pseudo-differential one with a specific nonlinear terms cancelation technique in order to prove that this technique is appropriate for a pseudo-differential topology, as well.

A negative resistance is used for further DC gain enhancement. The transconductance tuning for compensating the PVT variations, is achieved by a MOS transistor operating in the cut off region to provide large resistance for tuning, because small resistance adds more noise to the circuit. As an application of the proposed OTA, a third-order low-pass Butterworth filter is designed, which also operates as a VGA. It has a gain tuning from −1 to 23 dB by 6 dB gain steps.

The rest of the paper is organized as follows: the proposed OTA with circuit details and performance improvement techniques are described in Section 2. In Section 3, Gm-C filter and its gain tuning method is presented. Simulation results of the OTA and filter are presented in Section 4. Some discussion about the circuit simulations is made in Section 5. Finally, the conclusions are drawn in Section 6.

2. TRANSCONDUCTANCE DESCRIPTION

2.1. The proposed low voltage and linear cell

Figure 1 shows half circuit of the proposed bulk-driven pseudo-differential cell, which uses nonlinear terms cancelation technique for the linearity improvement. Because an n-well technology is considered and because the input differential signals should be applied to the bulks of the input transistors, PMOS transistors is considered for the input differential pair, which allows separate bulk voltages for the transistors. If bulk-driven NMOS transistors are used, they should be implemented in p-wells, and this would increase cost, because of the need for extra mask layers.

DOI: 10.1002/cta

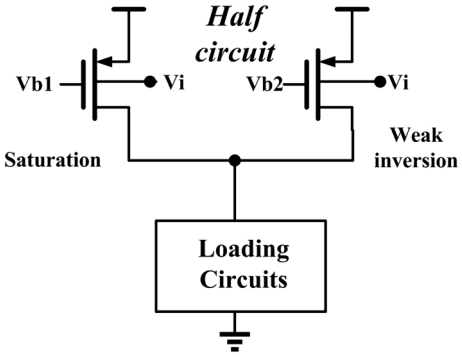

Figure 1. Half circuit of the proposed bulk-driven, pseudo-differential cell.

The linearity improvement technique is based on the fact that, transistors in saturation and weak inversion regions have opposite signs in the third-order harmonic distortion term. Because the ac signal is applied across the bulk-source junction, by taking nonlinear effects into account, the differential output current can be represented as:

$$I_0 = I_{D1} - I_{D2} = a_1 V_{BS} + a_2 V_{BS}^2 + a_3 V_{BS}^3 + \ldots \tag{1}$$

Because even-order harmonic distortion has been canceled out due to the differential structure, third-order harmonic distortion is the dominant term of nonlinearity, which can be calculate as follows:

$$|V_{th}| = |V_{th0}| + |\gamma|\left[\sqrt{2|\varphi_F| + V_{BS}} - \sqrt{2|\varphi_F|}\right] \tag{2}$$

The drain current and the third-order harmonic distortion term of PMOS transistors in the saturation region can be approximated by (3) and (4). In order to simplify the expressions, channel length modulation and velocity saturation effects are not considered.

$$I_{D,saturation} = \frac{\mu_P C_{ox} W (V_{SG} - |V_{th}|)^2}{2L} \tag{3}$$

$$a_{3,saturation} = \frac{\partial^3 (I_{D,sat})}{3!\partial (V_{BS})^3} = -\frac{\mu_P C_{ox} W \left(\gamma^2 \sqrt{2|\varphi_F|} + |\gamma|(V_{SG} - |V_{th0}|)\right)}{16L\left(\sqrt{2|\varphi_F| + V_{BS}}\right)(2|\varphi_F| + V_{BS})^2} \tag{4}$$

On the other hand, the drain current and the third-order harmonic distortion term of the weak inversion region transistors are expressed as [16]:

$$I_{D,weakinversion} = I_0 \left(\frac{W}{L}\right) e^{(V_{GS} - V_{th} - V_{off}/\zeta V_T)} \left(1 - e^{(-V_{DS}/V_T)}\right) \tag{5}$$

$$a_{3,weakinversion} = \frac{\partial^3 (I_{D,weak})}{3!\partial (V_{BS})^3} \approx \frac{(\zeta - 1)^3}{6\zeta^3} \frac{I_D}{{V_T}^3} \tag{6}$$

$$\zeta \approx 1 + \frac{\gamma}{2\sqrt{1.5\varphi_F + V_{SB}}} \tag{7}$$

$$a_{3,total} = a_{3,saturation} + a_{3,weakinversion} \tag{8}$$

DOI: 10.1002/cta

In the previous equations, φ_F is the surface potential, γ is the body effect coefficient, I_0 is the process dependent parameter, ζ is the weak inversion slope factor, V_T is the thermal voltage, V_{off} is a model parameter, and a_3 is the coefficient of the third-order harmonic distortion term. As can be seen from (8), by combination of the currents in the saturation and weak inversion regions and by choosing proper sizes for the input transistors and proper value for their biases, the total third-order harmonic distortion can be canceled out. In fact, under the conditions which force (8) to zero, the total third-order harmonic distortion can be properly eliminated.

2.2. *Circuit technique for the transconductance enhancement*

The proposed bulk-driven core, which is described in the previous section, has a low input transconductance, which leads to a low gain bandwidth, low DC gain, and high input referred noise. In fact, input transconductance is 2 to 5 times lower in the bulk-driven transistors in comparison with the gate driven ones, which results in some performance limitations. In the proposed low voltage, low power OTA, disadvantages of the bulk-driven transistors can be ignored in tradeoff with reduction in power and the supply voltage. But this major disadvantage should be compensated by some circuit techniques. Figure 2 shows the transconductance enhancement technique [19], which is accomplished by the active load. The flipped voltage follower current mirror is used for mirroring the current to the output. M3 implements a partial positive feedback and lowers the conductance of the node A. This technique increases g_{mb} by the η factor, as in the succeeding text.

$$\eta = \frac{1}{1 - \left(g_{m,M3}/g_{m,M4}\right)} \tag{9}$$

in which, $g_{m,\mathrm{M3}}$ and $g_{m,\mathrm{M4}}$ are gate transconductance of M3 and M4, respectively.

In order that the overall feedback remain negative, $g_{m,\mathrm{M3}}$ must be smaller than $g_{m,\mathrm{M4}}$. On the other hand, if $g_{m,\mathrm{M3}}/g_{m,\mathrm{M4}}$ is close to unity, the circuit is very prone to instability, and linear input voltage range becomes small. In fact, a tradeoff exists between linearity and increasing g_{mb}. So, appropriate circuit implementation could be achieved by proper sizing M3 and M4.

2.3. *Complete design of the proposed transconductance*

The complete OTA is shown in Figure 3, which consists of the transconductance main stage, the common mode feedback circuit (CMFB), the negative resistance, and the bias circuits. Because of the adequate common mode rejection ratio of the OTA (based on simulations), there is no need to a common mode feedforward circuit.

In Figure 3(a)–(d), all transistors with the same size are labeled with the same symbols. Because p–n junction current of the input transistors increases by temperature, the size and bias of the input transistors should be carefully selected to prevent high junction currents. In order to tune the transconductance value for compensating the PVT variations, a cutoff region transistor, which is referred to as the tuning transistor, is used (MR) to produce a large resistance. As using low

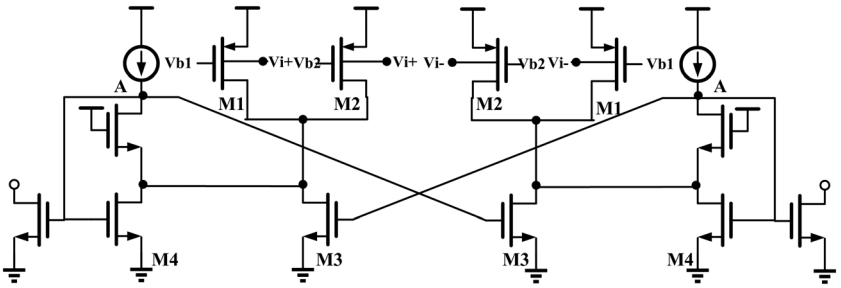

Figure 2. The transconductance enhancement technique.

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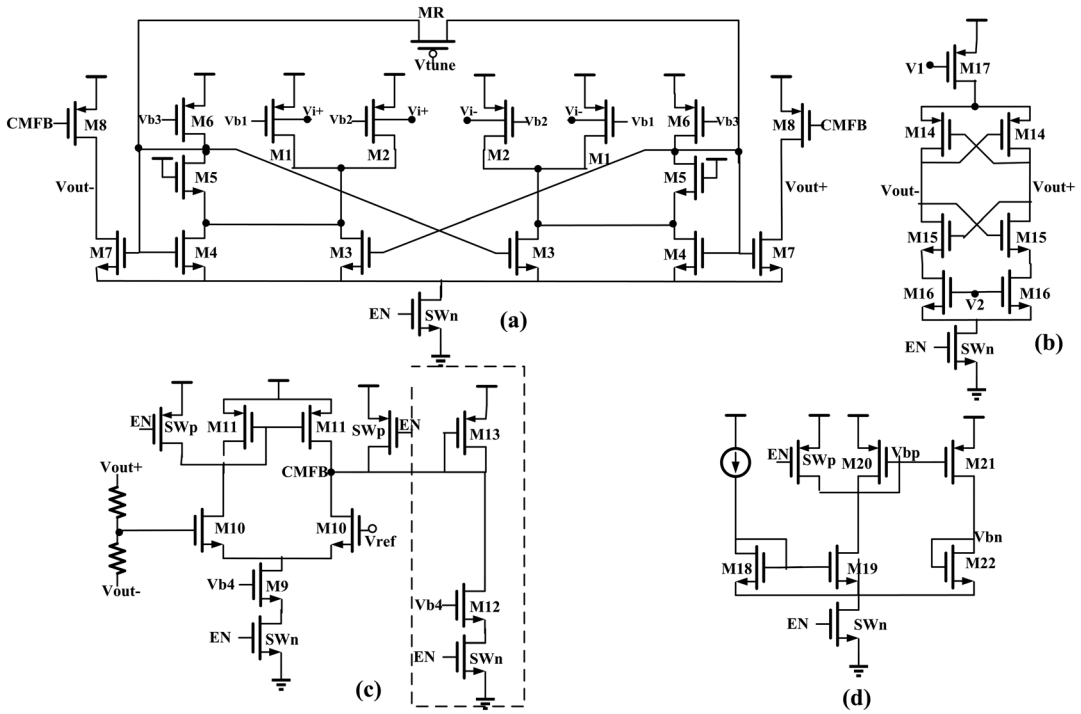

Figure 3. The complete operational transconductance amplifier (a) transconductance main stage, (b) negative resistance, (c) common mode feedback (CMFB) circuit, and (d) bias circuit.

resistance for tuning can cause large input referred noise, we have used a large resistance here [6]. By tuning the gate voltage of this transistor (Vtune), the transconductance value can be adjusted.

In the output stage, because of the low supply voltage, it is not possible to stack transistors for getting high output impedance. So, a complementary negative resistance circuit based on positive feedback is used to achieve higher output impedance. Figure 3(b) shows this negative resistance. V1 and V2 are used to prevent instability occurrence of the overall circuit due to the process variations and mismatch problems. So, mismatch effects is not important in this circuit. These voltages could be compensated with lookup table in the worst cases of instability that happen in high temperature conditions. Then these compensated voltages could be used in other conditions.

Figure 3(c) demonstrates the CMFB, which sets the output common mode to Vref. A resistive common mode detector is used for its high linearity. The output of the OTA is sampled with the resistive network, and the average of the differential outputs is compared with Vref and the resultant signal adjusts bias of M8, so that the output DC voltage is set around Vref. The circuit in the dashed line is the compensation circuit, which is used for high temperature conditions. Because the current of p–n junction grows in higher temperatures, when the OTAs are cascaded in the filter architecture, this increased current, draws the output currents of the connected OTAs, and reduces their output swing. In fact, this additional circuit changes the CMFB bias in order to produce more current in the output stage of the OTAs for recovering the drawn current.

Bias circuit is demonstrated in Figure 3(d). In this figure, Vbp and Vbn are used for biasing of PMOS and NMOS transistors, respectively.

In Figure 3, the transistors with SW labels are switches. The EN is a control signal that turns on and off the OTA for gain tuning of the filter (will be described in detail Section 3). When EN is high, the SWp and SWn switches are off and on, respectively. In this mode, the OTA acts normally. When EN goes low, SWn is turned off and thus no current path exists to ground. In this mode, SWp is also turned on to force PMOS biases to VDD (Power supply) and turn those transistors off. As a result, the OTA is disabled.

The transistor sizes chosen for the main stage of transconductance and their bias values are provided in Tables I and II, respectively . It should be noted that, the bias voltages are designed with the circuit in Figure 3(d).

DOI: 10.1002/cta

Table I. The transistor sizes for the main stage of transconductance.

Transistor	M1	M2	M3	M4	M5	M6	M7	M8	MR
(W/L)(μm/μm)	1.2/0.36	1.9/0.18	1.8/1.8	3.5/1.26	0.4/1.26	0.4/1.08	3.7/0.36	90/0.9	0.4/0.18

Table II. The bias values for the main stage of transconductance.

Bias voltage	Vb1	Vb2	Vb3
Value (V)	0.2	0.5	0.2

2.4. Noise in the proposed circuit

The noise performance of the proposed OTA is discussed in this section. The total input referred noise of the proposed OTA, which consists of thermal and flicker noise is derived as [6], [16] and [19]:

$$\begin{aligned}\overline{V_{n,in}^2} = &\left[2\frac{8KT}{3g_{mb}^2}(g_{m1}+g_{m2}+g_{m3}+g_{m4})\right]+\frac{2}{c_{ox}f}\frac{1}{}\left[\left(\frac{k_{fp,sat}\,g_{m1}^2}{(WL)_1 g_{mb}^2}\right)+\left(\frac{k_{fp,weak}g_{m2}^2}{(WL)_2 g_{mb}^2}\right)+\left(\frac{k_{fn,sat}\,g_{m3}^2}{(WL)_3 g_{mb}^2}\right)\right.\\ &\left.+\left(\frac{k_{fn,sat}\,g_{m4}^2}{(WL)_4 g_{mb}^2}\right)+\left(\frac{g_{m4}R_{MR}}{2+g_{m4}R_{MR}}\right)^2\left\{\left[2\frac{8KT}{3g_{mb}^2}(g_{m6})\right]+\frac{2}{c_{ox}f}\frac{1}{}\left[\left(\frac{k_{fp,sat}\,g_{m6}^2}{(WL)_6 g_{mb}^2}\right)\right]\right\}\right.\\ &\left.+\left[\left(\frac{g_{m4}R_{MR}}{2+g_{m4}R_{MR}}\right)^2\left(\frac{8KT}{g_{mb}^2R_{MR}}\right)\right]+\left[2\frac{8KT}{3\left(\frac{g_{m7}}{g_{m4}}\right)^2 g_{m,eff}^2}(g_{m7}+g_{m8})\right]\right.\\ &\left.+\frac{2}{c_{ox}f}\frac{1}{}\left[\left(\frac{k_{fn,sat}\quad g_{m7}^2}{(WL)_7\left(\frac{g_{m7}}{g_{m4}}\right)^2 g_{m,eff}^2}\right)+\left(\frac{k_{fp,sat}\quad g_{m8}^2}{(WL)_8\left(\frac{g_{m7}}{g_{m4}}\right)^2 g_{m,eff}^2}\right)\right]\end{aligned} \tag{10}$$

in which k_f is the flicker noise parameter, K is Boltzmann constant, T is the temperature, f is the frequency, and other parameters have their usual meanings. The factor of 2 refers to the two halves of the input stage and $g_{m,eff}$ is $\eta^* g_{mb,total}$.

On the basis of (10), although, the transconductance enhancement technique causes an increase in the noise contribution of M1–M4 and M6, the total input referred noise is decreased. In fact, when considering the input referred noise, this increase in the output noise is counteracted by the DC gain enhancing due to the effect of the partial positive feedback [19]. For example, the noises of M7 and M8 are reduced by this technique due to the DC gain enhancing. The noise is further reduced by minimizing the current of M6.

3. GM-C FILTER DESIGN

The low supply voltage OTA, which is designed in the previous sections, can be used for WSN applications as a channel select filter and VGA of the receiver. The main standard introduced for WSNs is IEEE 802.15.4 or ZigBee. This low power consumption standard aims at wireless sensing and control applications with low voltage and low data rates, including industrial and commercial uses, home automation, consumer electronics, and personal health care appliances. Because of the requirements of these articles, the sensors compliant to the ZigBee standard should be able to run for several months on just button cells or small batteries [20] and therefore should be low voltage and low power. The low supply voltage design guarantees that the sensors could operate for much

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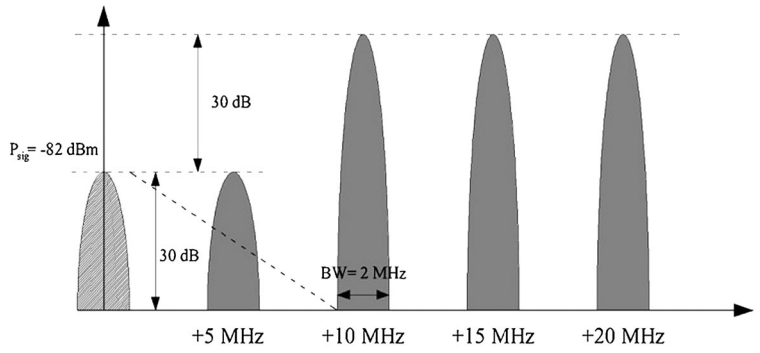

Figure 4. Channel selection in IEEE 802.15.4 standards [20].

more time and there would be no need for changing batteries as soon. In this paper, it is assumed that the architecture of the ZigBee receiver is zero-IF and it operates in the frequency band of 2.4 GHz, which is available throughout the world. Therefore, for selection of channels, a 2 MHz bandwidth low-pass filter should be used to meet the requirement of 0 dB rejection at the adjacent channel (±5 MHz) and 30 dB rejection at the alternate channel (±10 MHz), respectively as shown in Figure 4 [20]. Assuming some margins, a third-order Butterworth filter with cutoff frequency of more than 1 MHz can be used for this purpose [20]. In order to provide some gain controlling feature to the receiver, this filter is designed to operate as a VGA, as well.

The filter is based on the cascade of a first-order low-pass stage and another biquad stage for realizing a complex pole pair. The biquad structure is chosen because of its simplicity for gain tuning. By increasing the number of parallel g_m stages, the transconductance value enhances linearly, and gain tuning of the filter is achieved. The g_m value of the parallel transconductors could be tuned by the tuning transistor to obtain the required gain. Figure 5 shows the implementation of the filter. In this figure, some switches are used to vary the gain of the filter, which are controlled by the EN < i > signals. These switches are implemented by transistors. When EN < i > goes high, the related OTA is activated and enhances the g_m value and therefore the gain of the filter. In this figure, En < 1–5 > and EN < 1–4 > refer to the control for five and four g_m circuits that are switched on and off in parallel. The frequency response of the filter is as follows:

$$H(S) = \frac{g_{m1}/C}{s + g_{m2}/C} \frac{g'_{m1}g'_{m3}/C_AC_B}{s^2 + s\left(g'_{m4}/C_A\right) + g'_{m2}g'_{m3}/C_AC_B} = \frac{k_1}{s + 2\pi f_c} \frac{k_2}{s^2 + s\left(\omega_0/Q\right) + \omega_0^2} \tag{11}$$

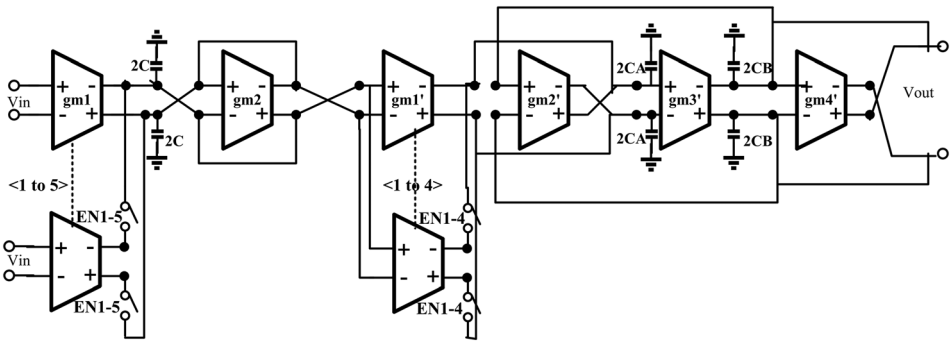

Figure 5. The implementation of the third-order low-pass filter.

DOI: 10.1002/cta

Where,

$$\omega_0 = 2\pi f_c\sqrt{\sigma^2+\omega^2}, Q = \frac{\sqrt{\sigma^2+\omega^2}}{2\sigma} \tag{12}$$

In the previous expressions, σ and ω represent the real and imaginary parts of the complex pole, respectively, f_c is the cut off frequency of the filter, K_1 and K_2 are the gain values and other parameters have their usual meanings. As can be seen from the previous expressions, by changing the transconductance value of g_{m1} and g'_{m1}, the gain of the filter can be tuned without any variation in the cutoff frequency.

4. SIMULATION RESULTS

4.1. Simulation results of the operational transconductance amplifier

The OTA and filter are simulated in a 0.18 μm n-well CMOS process. The OTA was designed to operate with a 0.8 V supply voltage. Simulations show power consumptions of 31.2 μW and 0.006 μW in on and off modes, respectively. The Vtune of the tunable transistor is tuned from 0 to 300 mV to compensate the transconductance value for the PVT (Process, Voltage, Temperature) variations. The transconductance tuning versus input voltage is demonstrated in Figure 6. The simulated THD for 400, 600, and 800 mV differential input signals at 1 MHz and Vtune of 200 mV is −61.8, −54.1, and −47.6 dB, respectively. Simulations show that the THD of the OTA versus input amplitude of less than 800 mV_{ppd} remains below −40 dB over the tuning range. The input referred noise of the proposed OTA at 1 MHz frequency is simulated as 301.1 $nV/\sqrt{Hz}$ for Vtune of 300 mV, which increase to 322.2 $nV/\sqrt{Hz}$ for Vtune of 0 mV. This noise value is measured in fully differential condition. Common mode rejection ratio of the OTA is simulated as 102.4 dB for Vtune of 200 mV. This value is achieved for a single-ended output, which will be much higher for differential outputs and seems very good for a pseudo-differential structure. Table III summarizes the simulated performances of the OTA. Table IV shows corner case simulations of the OTA. Process and temperature worst case performances of the proposed OTA are demonstrated in Table V, which shows proper operation of the OTA over process and temperature variations. Table VI compares the performances of the proposed OTA with recently published work. A figure of merit (FOM) as defined in [11] is used for the comparison as well, in which the transconductance value, linearity performance, speed of the circuit, input swing range, and power consumption are considered, as follows.

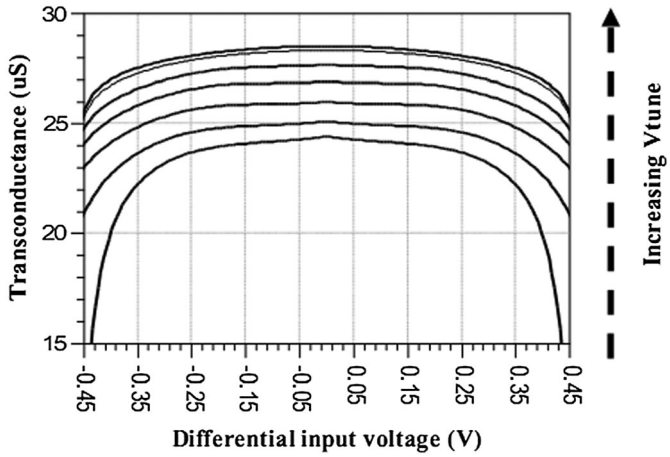

Figure 6. Transconductance tuning versus differential input voltage.

DOI: 10.1002/cta

Table III. Performance summary of the proposed operational transconductance amplifier.

Specification	Value
Technology	0.18 μm CMOS
Power supply	0.8 V
Power consumption(μW)	On mode = 31.2 Off mode = 0.006
THD (dB) @1 MHz (Vtune=200 mV)	−61.8, −54.1, −47.6*
Input referred noise @1 MHz in tuning range (nV/$\sqrt{\text{Hz}}$)	301.1–322.2
DC gain(dB)**	33
Unity gain bandwidth (MHz)**	7.8
CMRR(dB)**	102.4
PSRR+(dB)**	81
PSRR-(dB)**	27

THD, total harmonic distortion; CMRR, common mode rejection ratio; PSRR, power supply rejection ratio.
CMRR and PSRR values are reported for a single-ended output. Differential output values are much higher.
*At 400, 600, and 800 mV_{ppd} input signal, respectively,
**Cload = 1 pF and Vtune = 200 mV.

Table IV. Corner case simulations of the operational transconductance amplifier.

	TT	SS	SF	FS	FF
Power consumption (μW)	31.2 Off = 0.006	28.56 Off = 0.002	31.28 Off = 0.002	30.64 Off = 0.09	33.28 Off = 0.09
THD (dB) (600mV_{ppd} input signal)*	−54	−52.6	−42.8	52.3	−51.3
Input referred noise (nV/$\sqrt{\text{Hz}}$)*	301	318	325.3	308	289

*@1 MHz, Vtune = 200 mV

Table V. Process and temperature worst case performances of the proposed operational transconductance amplifier.

	Min	Typical	Max
Temperature (°C)	−40	25	60
Power consumption in on mode (μW)	28.4	31.2	35
THD (dB) for 600 mV_{ppd} input signal*	−63.8	−54	−39.2
Input referred noise (nV/$\sqrt{\text{Hz}}$)*	257.9	301	347

*@ 1 MHz, Vtune=200 mV

$$FOM = 10\log\frac{G_m \times V_{id} \times THD \times f_0}{P} \tag{13}$$

Although the FOM of our work is little lower than some other designs, if we include the effect of supply voltage in the design using FOM/VDD, it can be seen that the proposed OTA compares favorably with the others.

4.2. *Simulation results of the filter*

Frequency response of the third-order low-pass Butterworth filter with 1 MHz cut off frequency and −1 to 23 dB gain variation with 6 dB steps is represented in Figure 7. The proposed filter achieves attenuation of 32.8 dB at 5 MHz and 50.7 dB at 10 MHz for a 5 dB gain of filter. The filter is

DOI: 10.1002/cta

Table VI. Performance summary of the operational transconductance amplifier and comparison with recently published work.

Year	Tech.	VDD (V)	V_{ppd} (mV)	THD of output current (dB)	Power (W)	Input referred noise (nV/$\sqrt{}$Hz)	g_m Value (μS)	FOM	FOM/VDD
2007[6]	0.18 μm Gate driven	1	400	−70@1 MHz	2.5 m	13	1000	87	87
2008[11]	0.18 μm Gate driven	1.5	900	−60IM3@40 MHz OR −69.5 THD	9.5 m	23	470	97.2	64.8
2011[16]	0.18 μm Bulk driven	0.5	500	—	60 μ	80@1 MHz	—	—	—
2011[21]	0.18 μm Bulk driven	1	800	−55@1 MHz	70 μ Vtune=0.43 V	—	5.6	75.5	75.5
2005[22]	0.18 μm Bulk driven	0.5	—	−40@1 MHz	100 μ	90@1 MHz	—	—	—
This work	0.18 μm Bulk driven	0.8	800	−61.8, −54, −47.6**	31.2 μ	301 (Full diff)*	28.4	82.4	103

THD, total harmonic distortion; FOM, figure of merit.
*@1 MHz, Vtune=200 mV
**At 400, 600, and 800 mV_{ppd} input signal, respectively (@1 MHz, Vtune=200 mV)

DOI: 10.1002/cta

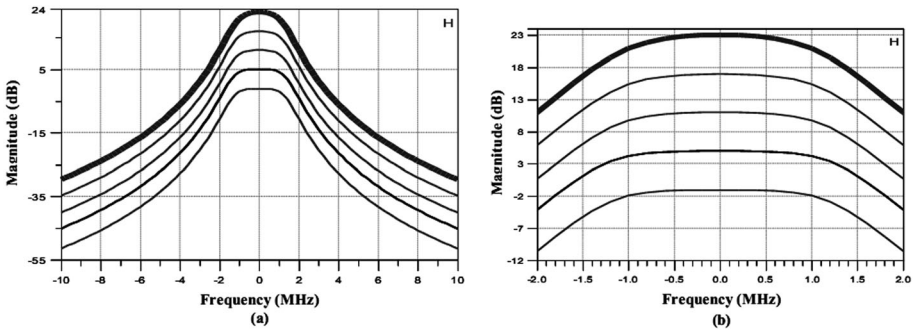

Figure 7. Frequency response of the third-order low-pass filter, (a) total response and (b) zoom in the passband of the frequency response.

designed for cutoff frequency of more than 1 MHz to ensure that the filter never removes desired signal power below 1 MHz bandwidth, because when the number of parallel g_m increases, the output impedance of the compound transconductors decreases, and this leads to a change in the transfer function of the filter (i.e., reduction of the filter bandwidth).

The filter consumes 187.2 to 405.6 μW power for gain tunings of −1 to 23 dB. The IIP3 of the filter at a 5 dB gain is calculated as shown in Figure 8 for the two input tones of 0.99 and 1.01 MHz. The in-band IIP3 is simulated to be 14 dBm referred to the 50 Ω impedance. The differential output swing of the filter, which leads to 1% THD is simulated as 0.58 V_{ppd} that seems good for a 0.8 V supply design. The simulated input referred noise of the filter is 165.8 nV/$\sqrt{\text{Hz}}$ at maximum gain, which increases to 826.6 nV/$\sqrt{\text{Hz}}$ at minimum gain of the filter. This high noise, which can be attributed to the bulk-driven transistors, low supply voltage, and low power consumption, could be improved by some noise cancelation techniques. In fact, this issue can be ignored in tradeoff with the reduced supply voltage and power consumption. The simulated performances of the filter are summarized in Table VII. Corner case simulations of the proposed filer are shown in Table VIII. Corner case and −40°C to 60°C temperature simulations of filter are performed also and show IIP3 better than −7 dBm at 5 dB gain of filter in worst case. This low IIP3 is related to the procedure that is used for the compensation of the negative resistance. The negative resistance is compensated at 60°C, which, based on the simulations, is the worst case for instability of the overall output impedance of the OTA. Then this compensated negative resistance is used at other temperatures, which results in lower output impedance and lower DC gain for those temperatures. If the negative resistance is compensated at all temperatures, much higher IIP3 would have been achieved.

Performance of the designed filter in comparison with the recently published similar work is reported in Table IX, which compares the proposed filter performances at a 5 dB gain with other work. For comparison, an FOM is used as well, as [23]

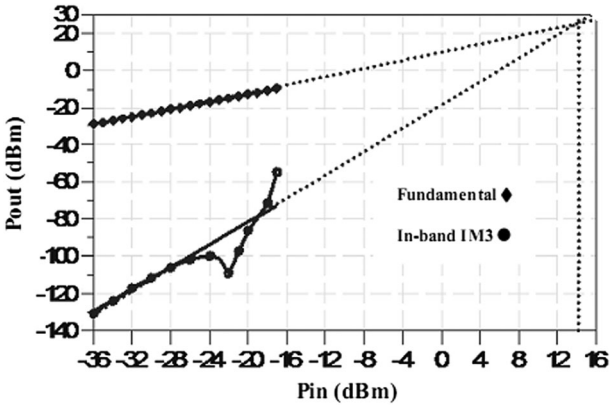

Figure 8. In-band IIP3 calculation for a 5 dB gain of filter.

DOI: 10.1002/cta

Table VII. Performance summary of the proposed filter.

Specification	Value
Technology	0.18 μm CMOS
Power supply	0.8 V
Filter type	Third-order low-pass Butterworth
Cut off frequency (MHz)	1
Gain tuning (dB)	−1 to 23
Attenuation at 5 dB gain of filter (dB)	32.8@5 MHz 50.7@10 MHz
Power consumption (μW)	187.2, 218.4, 405.6*
IIP3 (dBm)	16.5, 14, −9*
Input referred noise@1 MHz (nV/$\sqrt{\text{Hz}}$)	826.6, 443, 165.8*

*At −1, 5, and 23 dB gain of filter, respectively.

Table VIII. Corner case simulation results of the filter.

	TT	SS	SF	FS	FF
IIP3 (dBm)*	14	2	5	2	1.5
NF (dB)*	53.5	54	54	53.7	52.9
Output swing (V)	0.58	0.4	0.514	0.556	0.5 V
Cut off frequency (MHz)*	1.3	1.2	1.15	1.3	1.5
Attenuation(dB) at 5 MHz*	32.8	34.5	35	33	30
Attenuation(dB) at 10 MHz*	50.7	52.4	53	51	48

*@5 dB gain

$$FOM = \frac{\left(\frac{P_C}{N}\right)}{f_c SFDR N^{4/3}}, SFDR = \left(\frac{IIP_3}{P_N}\right)^{2/3} \tag{14}$$

in which, P_c is the power consumption of the filter, N is the number of poles and zeros, f_c is the cutoff frequency and the $SFDR.N^{4/3}$ expression is the normalized spurious free dynamic range [23]. Here, unlike the FOM defined for OTA, the lower the FOM, the better the design. For a better comparison, the average of FOM is used for the designs that have cutoff frequency tuning. Also, we have calculated FOM× VDD as well to take the effect of supply voltage into account. As shown in the table, the proposed low voltage filter compares favorably with others. Reference [23] that has a much better FOM× VDD performance has not tried to introduce a low voltage design; this design has used 1 V supply in 90 nm CMOS technology. We have used 0.8 V supply in 0.18 μm CMOS technology that is about 45% of full supply of 1.8 V. So, low voltage design issues, such as reduced linearity, are much more pronounced in our work.

5. DISCUSSION/ANALYSIS

A 0.8 V supply bulk-driven transconductance is designed in this paper. The tuning capability is added to the transconductance for compensating PVT variations and achieving gain tuning for a third-order low-pass Butterworth filter. By parallelizing of the transconductor blocks, further gain tuning of the filter is achieved, which leads to gain tuning of −1 to 23 dB of filter.

The transconductance and filter are simulated in a standard 0.18 μm CMOS technology. The OTA consumes 31.2 μW power and shows THD of −61.8, −54.1, and −47.6 dB for 400, 600, and 800 mV differential input signals at 1 MHz and Vtune of 200 mV, respectively. Filter consumes 187.2–405.6 μW power for gain tunings of −1 to 23 dB. The filter shows the differential output swing of 0.58 V_{ppd}, which leads to 1% THD. This seems good for a 0.8 V supply design.

DOI: 10.1002/cta

Table IX. Performance summary of the filter and comparison with recently published work.

Year	Technology/input structure	VDD (V)	Power consumption (W)	IIP3 (dBm)	Input referred noise(nV/$\sqrt{\text{Hz}}$)	Order of low-pass filter	Cutoff frequency (MHz)	FOM (fJ)	FOM× VDD
2011[23]	90 nm gate driven	1	4.35 m	21.7–22.1	(Diff) 75	6	8.1–13.5	0.02*	0.02*
2009[13]	0.18 μm gate driven	1.2	4.1–11.1 m	19–22.3	12-425	3	0.5–20	1.54*	1.85*
2011[16]	0.18 μm bulk driven	0.5	326 μ	—	171 (@1 MHz)	3	1.4–6	—	—
2009 [24]	0.5 μm gate driven	5	180 m	33	64 (@1 MHz)	3	10	0.766	3.83
This work	0.18 μm bulk driven	0.8	218.4 μ**	14**	(Diff) 443 @1 MHz**	3	1	0.49**	0.39**

FOM, figure of merit.
*Average of FOM
**@5 dB gain

DOI: 10.1002/cta

Simulations of process corners and temperature variations from −40°C to 60°C are included to forecast the operation of the proposed design after fabrication and shows proper stability in all corner case and temperature.

6. CONCLUSIONS

A low supply transconductance with bulk-driven input pairs is designed and simulated in this work. The linearity improvement is achieved with nonlinear terms cancelation technique, using two parallelized differential topologies with opposite signs in the third-order harmonic distortion terms of the output current. A transconductance enhancement technique is applied to the OTA, in order to compensate some drawbacks of using bulk-driven cell, such as low transconductance value, low DC gain, and high noise. The high noise drawback of the bulk-driven cell could be further reduced by some noise cancelation technique.

The proposed OTA is utilized to design a third-order low-pass Gm-C filter with gain tuning, which can be used as a channel select filter and VGA for WSN application.

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