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A new quantum-dot cellular automata fault-tolerant full-adder

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Abstract A novel fault-tolerant full-adder for quantum-dot cellular automata is presented. Quantum-dot cellular automata (QCA) is an emerging technology and a possible alternative for semiconductor transistor based technologies. A novel fault-tolerant full-adder is proposed in this paper: This component is suitable for designing fault-tolerant QCA circuits. The redundant version of full-adder is simple in structure and more robust than the standard style for this device. By considering two-dimensional arrays of QCA cells, fault tolerance properties of such block full-adder can be analyzed in terms of misalignment, missing and dislocation cells. In order to verify the functionality of the proposed device, some physical proofs are provided. The results confirm our claims and its usefulness in designing digital circuits.

Keywords Quantum-dot cellular automata · Full-adder · Fault-tolerant logic gates · Nanoelectronic circuits

1 Introduction

As the current CMOS technology is going to approach fundamental physical limits, there has been extensive research in nano-scale for the future generation ICs. Quantum-dot cellular automata (QCA) is one of the promising new technologies that not only gives a solution at nano-scale, but also it offers a new method of computation and information transformation [1,2]. The superior features of QCA over current CMOS VLSI devices along with the feasibility of designing logic gates, circuits, and massively parallel architectures indicate the potential of QCA as a promising novel computing paradigm. In the sense that it would potentially allow the implementation of massively parallel computing architectures which could outperform the current CMOS VLSI counterparts in every performance aspect, that is, integration density, power consumption, and speed, while also enabling new applications by overcoming inherent limitations of VLSI technology [3].

There are, however, several obstacles for a practical realization of QCA and exploiting full potential of this new technology. Here, it suffices to mention the following issues:

- The first major obstacle is the realization of QCA hardware capable of performing in room temperature. Current semiconductor technologies that are being considered for the QCA implementation would operate only in cryogenic temperatures due to the large size of the cells. This, in turn, has motivated the investigation of molecular realization of QCA. The smaller size of molecules means that Coulomb energies are much larger, so room temperature operation is possible. In fact, there are indicates that realization of QCA-based molecular devices capable of functioning in the current commercial regime is possible. It should be mentioned that the focus of our work is on electronic realization of QCA devices as opposed to magnetic realization. It has been demonstrated that magnetic quantum dots, despite their large size, can operate at room temperature. In Sect. 2.2, we present a brief overview of the QCA implementation.
- The second obstacle is the means by which input state is fixed and the output state is measured. Obviously, the issue of connecting the nano-world to the micro-world is one that is germane to all type of nano-devices.
- The third issue is the required precision in the assembly and tolerance to fabrication defect. In fact, it is widely

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believed that QCA devices and circuits will highly sensitive to imprecision in their assembly. Here again it seems that molecular implementation provides an additional advantage by allowing the use of various self-assembly techniques. However, there are still questions as to whether molecular self-assembly techniques would give sufficient control over cell positioning.

In this letter, we will not address the first and second item. We will focus on an approach to overcome some of the issues related to the third item. Note that, the issue of fault tolerance has been so far analyzed from an implementation technology point of view. However, in this paper we study the issue of fault tolerance from an architecture point of view. Our approach is based upon considering two-dimensional arrays of QCA cells. Assuming a certain amount of blocks in the assembly of the QCA cells, it is still possible to design circuits that perform the desired functions despite their faulty assembly. This is the direction that we have been pursuing for enabling fault tolerant QCA full-adder.

Two fundamental units of QCA based design are majority and inverter gates; hence, efficient construction of QCA circuits using majority and inverter has attracted a lot of attention [4–14].

A single-bit full-adder can be implemented by using only majority and inverter gates [2]. As full-adder is the principle element of the arithmetic systems, its performance directly affects the performance of the entire system. Hence, efficiently constructing a full-adder in QCA is of great importance [4,10–12,15–17].

Fault-tolerant design of QCA logic circuits is absolutely necessary for characterization of defective behavior of QCA circuits. In recent years the fault tolerance properties of QCA circuits has been demonstrated by many researchers [3,6–9,18–23].

As already mentioned, full-adder is the basic element of QCA circuits; this note investigates a new design for fault-tolerant full-adder that offers remarkable robustness with respect to misalignment, missing and dislocation cells. The presented methods justified based on some physical models. Improving the robustness of the full-adders leads to efficient designing of many fault-tolerant arithmetic circuits.

2 Materials and methods

2.1 Review of QCA

Quantum cellular automata is a new device architecture, which is proper for the nanometer scale. The principle of QCA was proposed by Lent and Tougaw [24]. The basic computational element in QCA is a quantum cell. A quantum cell can be viewed as a set of four charge dots, positioned at the corners of a square. The cell contains two extra mobile electrons, which are allowed to tunnel between neighboring sites [2,25]. The electrons are forced to the corner positioned by columbic repulsion. The two possible polarization states represent logic "0" and "1" as shown in Fig. 1a [2,26].

As shown in Fig. 1b, an ordinary QCA majority gate requires only five QCA cells; three inputs labeled A, B and C, the device cell and the output. The logic function of majority gate is:

$$\mathrm{M(A,B,C)} = \mathrm{AB} + \mathrm{AC} + \mathrm{BC} \tag{1}$$

As illustrated in Fig. 1c, each single-bit full-adder can be implemented with only inverters and majority gates. The device has three inputs: two operands A, B, and the previous carry result C_{in}. The two outputs are the sum S and the carry bit C_{out}. Full-adders can be easily chained together to produce a multi-bit adder. And in Fig. 1d a QCA inverter is shown.

As stated earlier, a QCA array performs computation through Columbic interaction among neighboring cells that causes them to influence each other's polarization. Therefore, computation with QCA arrays is edge driven, in the sense that both energy and information flow in from the edges of the array only. This also provides the directionality in the computation by the array. In this sense, the difference between input and output cells is simply that inputs are fixed while outputs are free to change [24]. The QCA array then performs the desired computation by reacting to the change in the boundary conditions. The fact that the computation is edge driven implies that no direct contacts to interior cells are made and thus eliminating the interconnection problem. This further implies that the paradigm involves computing with ground states. That is, the QCA array reacts to change in the input and settles to a new ground state, which represents solution of the desired computational problem for which the array is specifically designed. However, computing with ground state implies that the computation is temperature sensitive. In fact, if the thermal fluctuations excite the array above its ground state then the array may produce wrong results. Furthermore, the dynamics of the array is hard to control. Consequently, the setting time to the ground state cannot be controlled or predicted and it would vary depending on the complexity of the array. Also, the array might settle to a stable state, producing wrong result or leading to a significant delay in reaching the true ground state.

In order to overcome these limitations of computing with ground state, a switching scheme has been developed [26]. In this scheme, a QCA array is divided into sub-arrays and a different clock controls each sub-array. The proposed clock scheme for QCA is multi-phased. This clocking scheme allows a given sub-array to perform its computation, have its state frozen by raising its inter-dot barriers, and then have its output as the input to the successor sub-array. Due to the

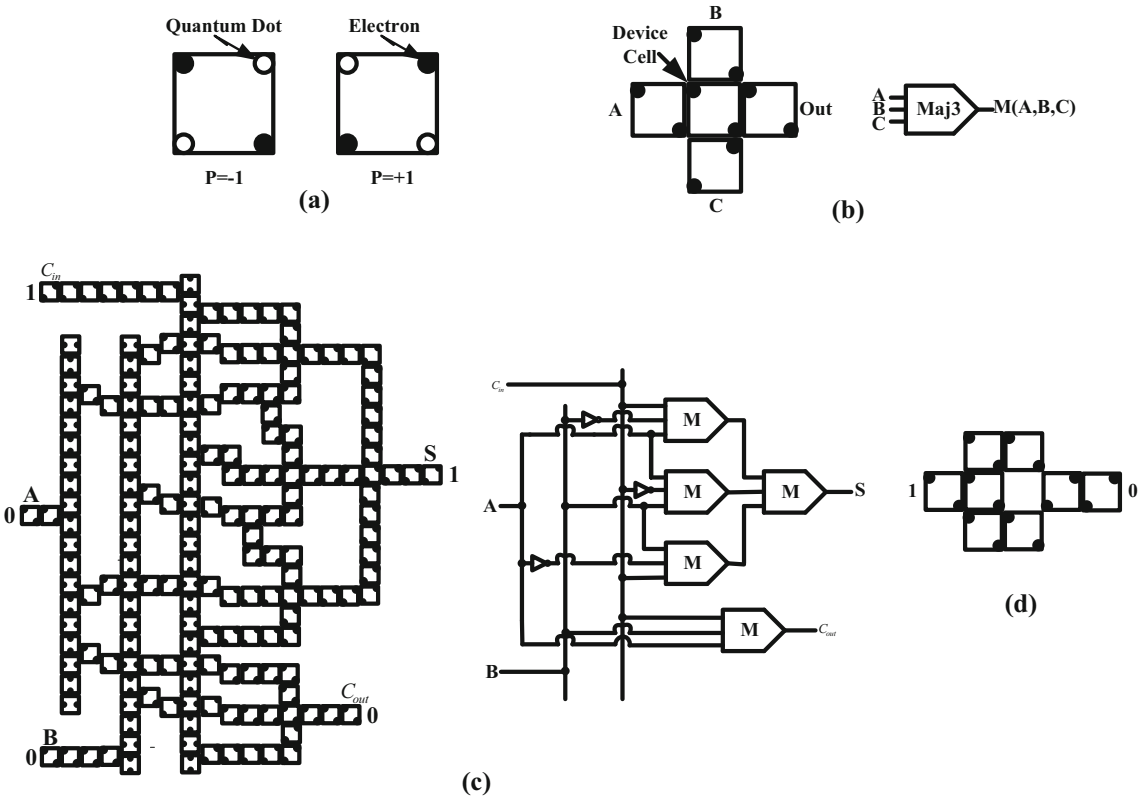

Fig. 1 **a** Basic QCA cell and binary encoding, **b** A three-input majority gate, **c** A single-bit full-adder **d** A QCA inverter

multi-phase nature of this clocking scheme, the successor sub-array is kept in an unpolarized state so it does not influence the calculation of preceding sub-array. Such clocking scheme implies a pipeline computation since different sub-array can perform different parts of the computation. In this sense, QCA arrays are inherently suitable for pipeline and systolic computation.

2.2 QCA implementation

There have been several proposals for physically implementing QCA [2,26–32]. In this section, a brief background on metal, molecular, and magnetic QCA is provided:

2.2.1 Metal QCA

Micro-sized QCA devices have been fabricated with metal. This device is composed of four aluminum islands (as dots) connected with aluminum oxide tunnel junctions and capacitors. The area of the tunnel junctions determines the island capacitance (the charging energy of the dots) and hence, the operating temperature of the device. The device has been fabricated using Electron Beam Lithography (EBL) and dual shadow evaporation on an oxidized silicon wafer. Experiments have confirmed that switching of electrons in a cell can control. A semiconductor implementation of QCA is advantageous due to well understood behavior of existing semiconductors for which several tools and techniques have been already developed. However, fabrication processes are not suitable to mass produce QCA cells of sufficiently small dimensions for operating at room temperature.

2.2.2 Molecular QCA

As an alternative technology, molecular QCA has several advantages over metal dot QCA; small cell size (density of up to 10^{13} devices per cm^2), a simple manufacturing process, and operation at room temperature are some of the desirable features of molecular QCA. Moreover, an improvement of switching speed by 100 times in molecular-sized QCA cells has been reported over semiconductor QCA cells. A further advantage of molecular QCA is that cells are structurally homogeneous down to the atomic level. In initial analysis of a simple molecular system, each molecule functions as a QCA cell and redox centers act as "quantum dots" in which information is encoded with charge configurations and tunneling is provided by bridging ligands. Some experiments suggest using nonbonding orbitals (π or d) as dot sites for a QCA molecule. Two, three, or four dot molecules have been fabricated. For example, the Trans-Ru$(dppm)_2$ $(C \equiv$

CFc) ($NCCH_2CH_2CH_2NH_2$)dication is a two redox center molecule that has been synthesized and attached on a silicon substrate [32]. The quantum dots in the molecules are ferrocenc Ru$(dppm)_2$ groups, while the tunneling junction for the mobile electron is provided by the carbon-carbon triple bond. Two molecules form a four-dot QCA cell.

2.2.3 Magnetic QCA

In magnetic implementation of QCA (MQCA), magnetostatic interactions between nanoparticles ensure that the system is bistable. The moments of the nanoparticles point either parallel, or anti-parallel with the axis of the chain, Information is propagated via magnetic exchange interactions as opposed to the electrostatic interactions in metal and molecular implementations. Experiments show that MQCA using relatively large dots (about 100 nm in size) operates at room temperature. MQCA provides the advantage of operation at room temperature even with current fabrication techniques. However, magnetic QCA does not appear to have the switching speed to compete with today's computers.

2.3 Advantages and difficulties of QCA-based design

QCA offers several distinct advantages over traditional technologies: (1) This schema inherently allows for very small feature size and thus high computational density. (2) Because current does not flow through QCA-based circuits, these designs can operate at very low power levels. This low power cost is vital to being able to achieve the device densities. (3) QCA design support massively parallel computational architectures, which can allow for more efficient information processing.

Many obstacles must be overcome before QCA-based circuits are available as a viable technology: (1) quantum cells must be small, on the order of 18nm, to be efficient. Currently the technology does not exist to reliably manufacture quantum cells of this size and assemble them into particular structures. Fortunately much time and effort is being spent on these scale related issues. (2) As with any technology on this scale, it is difficult to create interfaces between the computational circuits and I/O devices such as monitors and keyboards that would allow the user to interact with the computer. Also this limitation is face by other technologies. (3) QCA structures exhibit propagation delays. This delay can be attributed to the finite amount of time that it takes for the electrons in a cell to tunnel to their new position [7].

In addition to robustness capabilities of any future QCA device, another difficulty in its practical implementation is patterning a circuit. That is, if a simple gate is used within a QCA circuit then a high degree of accuracy is needed for proper alignment of cells. With today's technology, it is very hard to assemble a specific pattern, let alone making it precise. This issue should also be considered in the context of another problem associated with the manufacturing of massive arithmetic circuits. It is believed that QCA architectures could eventually be implemented with self-assembled molecules, although there are no candidates as yet and there are questions to whether molecular assemblies would give enough control over cell positioning [3]. This suggested that, while great QCA array with a very large number of cells can be implemented, the exact position of cells would be hard to control. In other words, practical implementation QCA array would represent a high degree of fault in cell positioning.

This has motivated us to investigate the design of QCA devices from a different perspective. In fact, instead of analyzing the behavior of a single cell, we have analyzed the behavior of two-dimensional arrays of cells for designing fault-tolerant QCA device.

2.4 Faults and fault tolerance

Three major categories of faults can occur during the assembly of a QCA circuit. First, faults may occur when quantum cells are shifted from their intended locations which are called "misalignment" cells. Sometimes misalignment cells have no effect on functionality of a QCA circuit, and also sometimes they can cause a circuit to have an unexpected output. A second type of faults occurs when the quantum cell itself is "missing" resulting in the cell becoming defective and it would have no influence on its neighbors and it can cause a circuit to cease functioning well. A third type of faults occurs when quantum cells are rotated relative to the other cells in the array which is called "dislocation" cells. Also, in this case, the circuit may cease to function.

Figure 2a shows misalignment cell in a full-adder. Obviously, due to symmetric, the direction of the cell movement is not important and it may cause the design does not function as a full-adder. In Fig. 2b, a missing cell in full-adder is presented that the design may cease to function. As shown in Fig. 2c, the dislocation cell with 45° rotation angle, also can cause a full-adder to have unexpected output.

Based on the researches which have been performed to date, some fault-tolerant QCA circuits have been with faults. In next section, we have attempted to make a novel fault-tolerant full-adder using physical relation; in such a manner that it can continue to operate correctly in the event of the above mentioned faults.

3 Fault-tolerant full-adder

The basis of functioning of the full-adder can be easily understood by considering Coulomb interaction among four neigh-

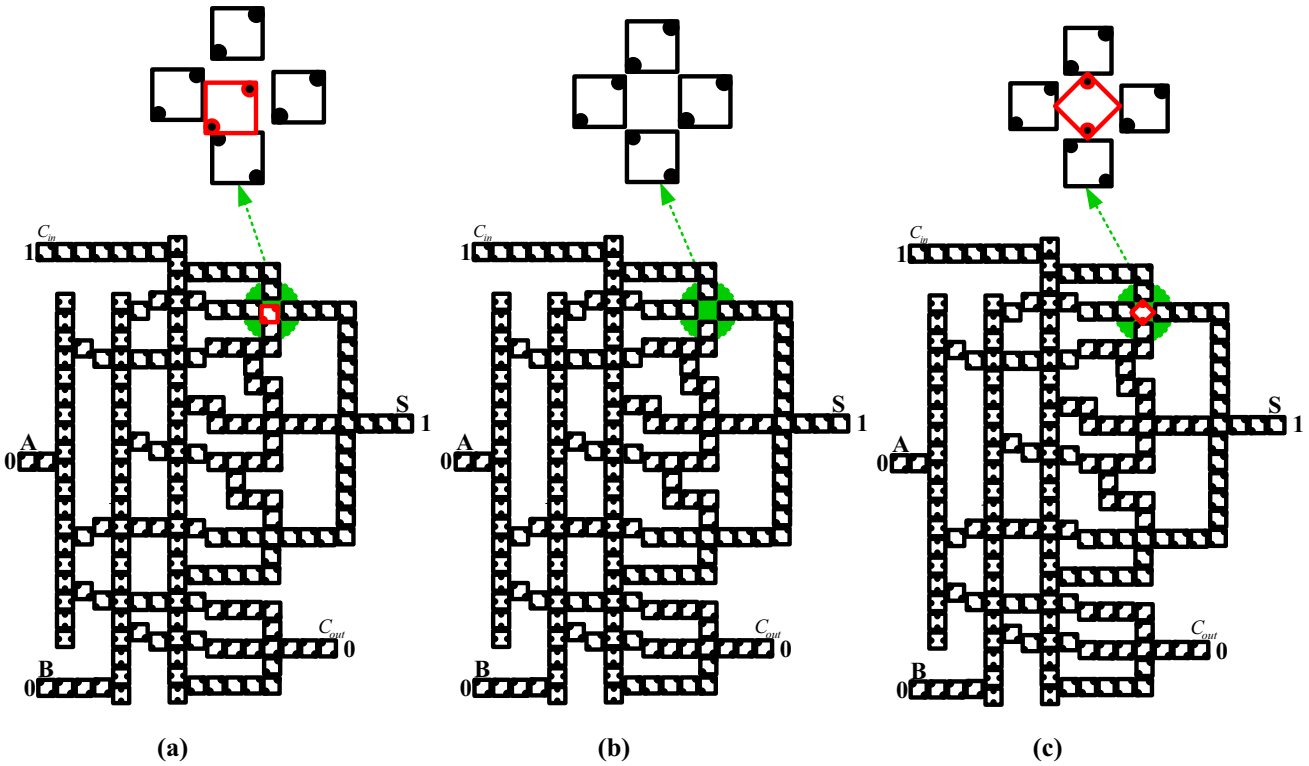

Fig. 2 Faults of single-bit full-adder, **a** misalignment cell, **b** missing cell and **c** dislocation cell

boring QCA cells. However, this also suggested that the correct function of such a device would strongly depend on the precision and geometry of its implantation. In order to assess the impact of the precision and geometry, we have studied and validated various configurations for implementation of the full-adder. This validation is performed by some physical relations using kink energy.

The novel proposed design for fault-tolerant full-adder is shown in Fig. 3. Here, the inputs are inserted from one side of the scheme and the outputs are measured at the other side. In this new structure, a fault-tolerant full-adder can be implemented only with fault-tolerant majority and inverter gates. In this scheme we have three inputs labeled A, B and C_{in} and two output cells are shown by S and C_{out}. In addition, five block 9th middle cells labeled Block1, Block2, Block3, Block4 and Block5 and twelve block 4th middle cells labeled 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 and 12. Polarization of input cells is fixed and middle cells and output cells are free to change. The rest of cells are considered as wire.

The property of the blocks is depending on number and position of device cells in each block. These remarkable collective of QCA cells are important from robustness point of view and they may also alleviate some of the problems related to patterning circuits.

The proposed design is based on majority and inverter blocks that allow several paths of information travel between inputs and outputs. This design allows some faults to be cancelled out by cells in blocks that are in correct state.

The presented scheme is justified based on physical relations.

Regarding the physical proofs, assume that all cells are similar and the length of each one is ($a = 18nm$) and there is a space of x ($x = 2nm$) between each two neighbors.

In all figures, rectangles show a QCA cell and the circles inside show the electrons within that cell. It should be noted that in order to achieve more stability, electrons of QCA cell are arranged in such a manner that reaches minimum kink energy (the difference in electrostatic energy between the two polarization states).

The kink energy between two electron charges is calculated using Eq. (2a). In this equation, U is kink energy, k is fixed colon, q_1 and q_2 are electric charges and r is the distance between two electric charges. By putting the values of k and q, we obtain Eq. (2b). U_T is the summation of kink energies that is calculated from Eq. (3) [33].

$$U = \frac{kq_1q_2}{r} \tag{2a}$$

$$k_{q_1q_2} = 9 \times 10^9 \times (1.6)^2 \times 10^{-38} = 23.04 \times 10^{-29} = A = cte \tag{2b}$$

$$U_T = \sum_{i=1}^{2} U_i \tag{3}$$

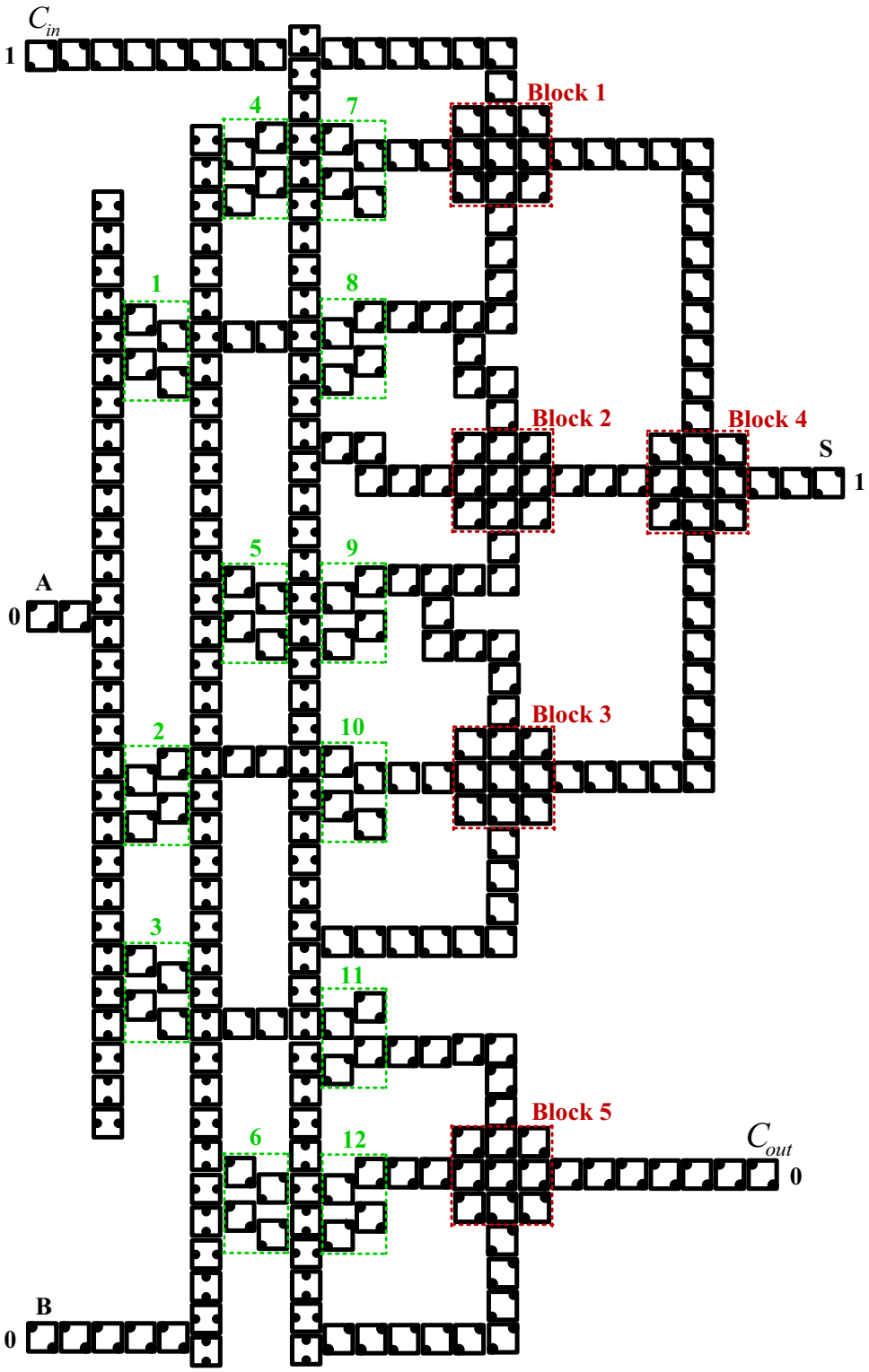

Fig. 3 Proposed fault-tolerant full-adder

The computation of the outputs requires five levels of blocks, thus the total latency of the outputs is five clock phases. The design forms a multi-stage pipeline, which can compute in parallel.

3.1 Physical proof

As the proposed design has 93 different middle cells, we should check all the faults that may occur in middle cells

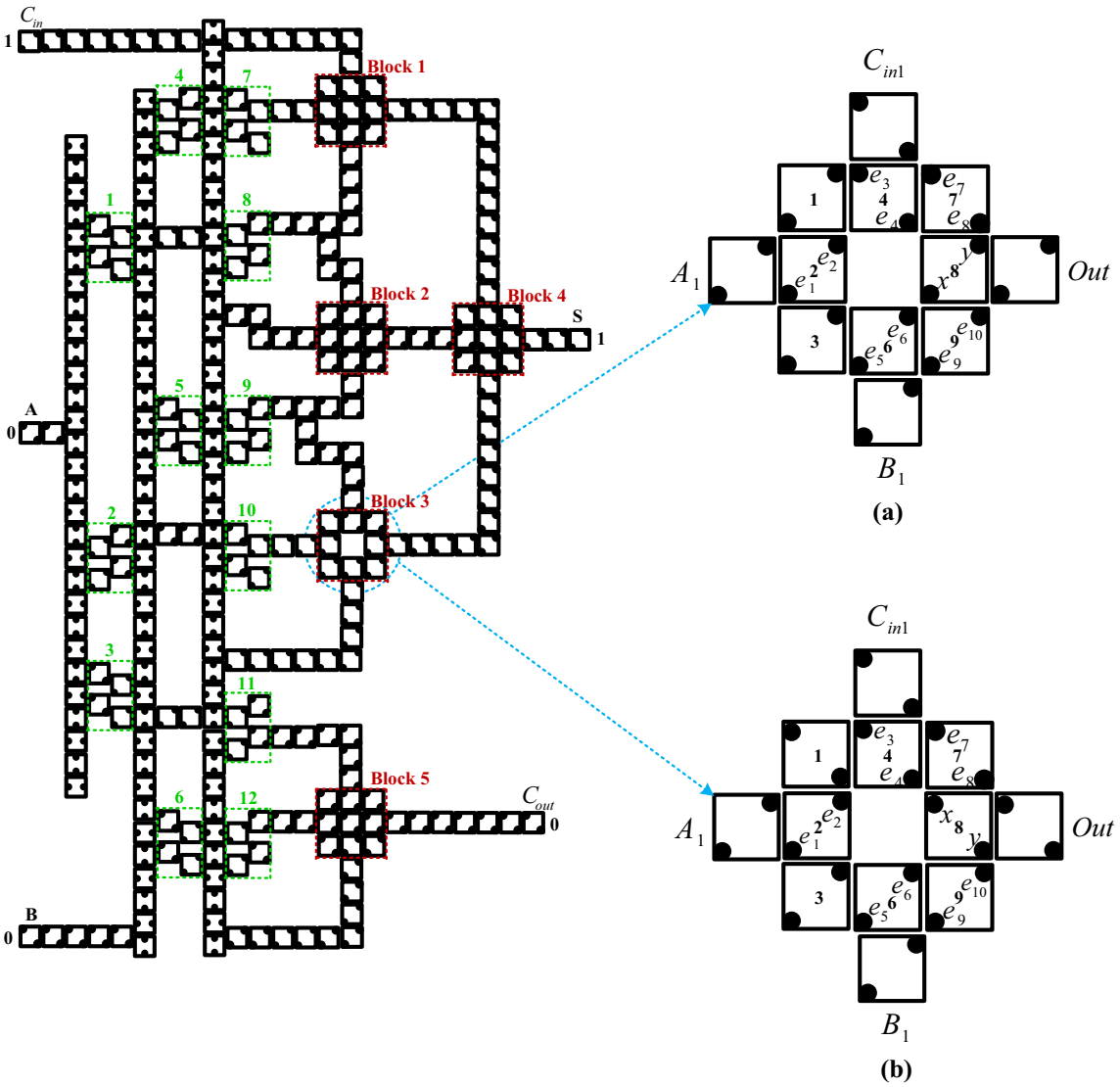

Fig. 4 **a** The one value in cell 8. **b** The zero value in cell 8

to verify the correctness of this scheme. Here, only one of the faults (missing cell 5 in Block3) is proved and the others can be proved as well. The assumed value of input cells are A = B = 0 and $C_{in} = 1$.

First, we calculate the kink energy existing between each electron ($e_1, e_2, e_3, e_4, e_5, e_6, e_7, e_8, e_9$ *and* e_{10}) with electrons "x" and "y" in (a) and (b) states using (2a) and (2b) equations. For example U_i is the kink energy existing between electrons e_i and x (or y). Also, r_i is the distance between two electron charges. Then we calculate the total kink energy (U_T) in both states using Eq. (3). The comparison of total kink energies in both (a) and (b) states shows that which state (a or b) is more stable. We consider the state that has the lower kink energy level as the more suitable one.

By considering the value of input cells we can gain the value of input cells for Block3 ($A_1 = B_1 = 1$ and $C_{in1} = 0$).

As the proof method is similar for all cells and their values and also due to lack of space, only the first part of this proof is stated and the rest of relations are omitted (Fig. 4).

Since cells 1 and 3 are roughly in a long distance from cell 8, their kink energy can be neglected. It should be noted that the value of cell 8 is transferred to the output cell (*Out*), which give us a majority decision of inputs A_1, B_1 and C_{in1}.

With comparison of the achieved results, the electrons in cell 8 are positioned in state (a) which is more stable and has lower kink energy. It is worth mentioning that in all cells U_{T_1} is the kink energy in +1 polarization and U_{T_2} is the kink energy in -1 polarization.

Figure 4a (electron x)

$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{40\times10^{-9}} \approx 0.58 \times 10^{-20}(J)$

$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{28.42\times10^{-9}} \approx 0.81 \times 10^{-20}(J)$

$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{42.94\times10^{-9}} \approx 0.54 \times 10^{-20}(J)$

$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{20.1\times10^{-9}} \approx 1.15 \times 10^{-20}(J)$

$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{28.28\times10^{-9}} \approx 0.81 \times 10^{-20}(J)$

$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{2.83\times10^{-9}} \approx 8.14 \times 10^{-20}(J)$

$U_7 = \frac{A}{r_7} = \frac{23.04\times10^{-29}}{38\times10^{-9}} \approx 0.61 \times 10^{-20}(J)$

$U_8 = \frac{A}{r_8} = \frac{23.04\times10^{-29}}{26.91\times10^{-9}} \approx 0.86 \times 10^{-20}(J)$

$U_9 = \frac{A}{r_9} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.15 \times 10^{-20}(J)$

$U_{10} = \frac{A}{r_{10}} = \frac{23.04\times10^{-29}}{18..11\times10^{-9}} \approx 1.27 \times 10^{-20}(J)$

$U_{T_{11}} = \sum_{i=1}^{10} U_i = 15.92 \times 10^{-20}(J)$

$U_{T_1} = \sum_{i=1}^{2} U_{1i} = 33.89 \times 10^{-20}(J)$

Fig. 4a (electron y)

$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{60.73\times10^{-9}} \approx 0.38 \times 10^{-20}(J)$

$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{40\times10^{-9}} \approx 0.58 \times 10^{-20}(J)$

$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{42.94\times10^{-9}} \approx 0.54 \times 10^{-20}(J)$

$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{20.1\times10^{-9}} \approx 1.15 \times 10^{-20}(J)$

$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{53.74\times10^{-9}} \approx 0.43 \times 10^{-20}(J)$

$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{28.28\times10^{-9}} \approx 0.81 \times 10^{-20}(J)$

$U_7 = \frac{A}{r_7} = \frac{23.04\times10^{-29}}{26.91\times10^{-9}} \approx 0.86 \times 10^{-20}(J)$

$U_8 = \frac{A}{r_8} = \frac{23.04\times10^{-29}}{2\times10^{-9}} \approx 11.52 \times 10^{-20}(J)$

$U_9 = \frac{A}{r_9} = \frac{23.04\times10^{-29}}{42.05\times10^{-9}} \approx 0.55 \times 10^{-20}(J)$

$U_{10} = \frac{A}{r_{10}} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.15 \times 10^{-20}(J)$

$U_{T_{12}} = \sum_{i=1}^{10} U_i = 17.97 \times 10^{-20}(J)$

Figure 4b (electron x)

$U_{T_{21}} = \sum_{i=1}^{10} U_i = 16.1 \times 10^{-20}(J)$

$U_{T_2} = \sum_{i=1}^{2} U_{1i} = 38.03 \times 10^{-20}(J)$

Fig. 4b (electron y)

$U_{T_{22}} = \sum_{i=1}^{10} U_i = 21093 \times 10^{-20}(J)$

Table 1 Single defective cell in proposed scheme

Defective cell no.	Out	Defective cell no.	Out
None	M(A,B,C)	1	M(A,B,C)
2	M(A,B,C)	3	M(A,B,C)
4	M(A,B′,C)	5	M(A,B,C)
6	M(A,B,C′)	7	M(A,B,C)
8	M(A,B′, C′)	9	M(A,B,C)

By considering middle cells in Block 3 (Fig. 3) the results are summarized in Table 1.

The following observation can be made from Table 1:

1. In all cases, proposed schemes with single defective cell function as the majority function or majority like function (majority function with one or two complemented variables).
2. Defective cell occurring corner cells (cells 1, 3, 7 and 9) does not change the logic function of block3, thus confirming the none-defect tolerant design of a single-bit full-adder.
3. Whenever cell 8 is defective, the polarization level experiences a drop (about ±0.1), but it also acts as majority gate. In all blocks, the total average of maximum polarization level decreased by increasing the number of defective cells.
4. Since the schemes Block1, Block2, Block3, Block4 and Block5 are similar to each other as well as schemes 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 and 12, one of the significant specifications of the proposed design is that it can tolerate multi-faults. For instance, if one of the mentioned faults in "Faults and Fault tolerance" section simultaneously occurs in Block1, Block2 and Block3 or 1,2 and 3 schemes, the proposed structure will still perform proper operation; that can be proved by physical relations.

Considering the above computing, we can infer that the proposed structure for implementing a fault-tolerant full-adder is correct and resulted in a correct state for the output cell when some faults occur.

Our study demonstrated the potential of this new approach to the design of fault-tolerant QCA arithmetic circuits. These results indicate the superior fault tolerance properties of QCA arrays in terms of misalignment, dislocation and missing cells. The next question is whether such proposed design can be implemented. As the first step toward this end, the parallel blocks are distinguishing by the fact that different clocks drive them in a pipeline fashion. Note that the whole edge of the first array is used as the input to the second blocks. In fact, a given QCA circuit can be divided into a set of smaller sub-arrays by assigning different clock to each sub-array. In such a circuit, each sub-array can perform a logic function similar to or different from other sub-arrays and the output of each sub-array is used as input to other sub-arrays.

4 Conclusion

A novel fault-tolerant full-adder for quantum-dot cellular automata is presented first in this paper. High performance logic component can be achieved by utilizing this fault-tolerant full-adder. Some physical proofs have verified the functionality of the presented structure. The proposed design demonstrates significantly more robust than the standard full-adder to single or multi-faults in misalignment cells, missing cells and dislocation cells and thus the difficulty in its practical usage that motivate further studies in this issue.

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