

Integrated Active Rectifier and Power Quality Compensator with Reduced Current Measurement

A. D. le Roux, J. A. du Toit, and J. H. R. Enslin, *Senior Member, IEEE*

Abstract—This paper describes a three-phase integrated active rectifier and shunt power quality compensator (IPQC). The measurement of only three currents is required, and the control algorithm can be implemented using a low-cost controller. The IPQC improves the harmonic content of the supply current, displacement power factor, supply current balance, and can serve as a four-quadrant active rectifier for motor drives and other dc-link loads. The operation of the IPQC is experimentally verified using a conventional three-phase insulated gate bipolar transistor voltage-source inverter. A low-cost fixed-point digital-signal-processor-based controller with fixed-band hysteresis current regulation is used for the implementation of the control algorithms.

Index Terms—Active power filter, active rectifier.

NOMENCLATURE

i_{NL}	Nonlinear load current [A].
i_{DL}	DC-bus (drive) load current [A].
i_C	Compensating current [A].
i_S	Supply current [A].
i_{LN}^A	Nonlinear load current active component [A].
i_C^A	Compensating current active component [A].
i_S^A	Supply current active component [A].
i_{CT}	Capacitor center-tap current [A].
G_T	Total load conductance [S].
G_{NL}	Nonlinear load conductance [S].
G_C	Compensator load conductance [S].
V_S	Supply phase voltage at the point of common coupling [V].
v_E	Filtered dc-bus voltage error [V].
V_{DC}^*	DC-bus voltage reference [V].
V_{DC}	DC-bus voltage [V].
V_{C1}	Top-capacitor voltage [V].
V_{C2}	Bottom-capacitor voltage [V].
$i_{Sa}^*, i_{Sb}^*, i_{Sc}^*$	Supply current references [A].

I. INTRODUCTION

A PLANT MAY contain one or more motor drives, with an active or passive rectifier, and other harmonic loads.

Manuscript received November 11, 1997; revised February 2, 1998. Abstract published on the Internet March 1, 1999.

The authors are with the Department of Electrical Engineering, University of Stellenbosch, Stellenbosch, 7602 South Africa (e-mail: jhenslin@firga.sun.ac.za).

Publisher Item Identifier S 0278-0046(99)04129-5.

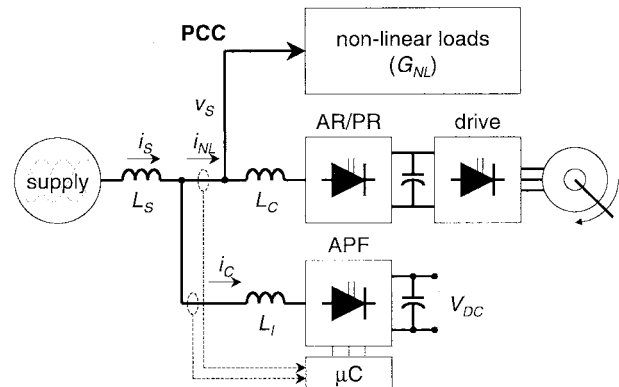


Fig. 1. Conventional power quality compensation strategy.

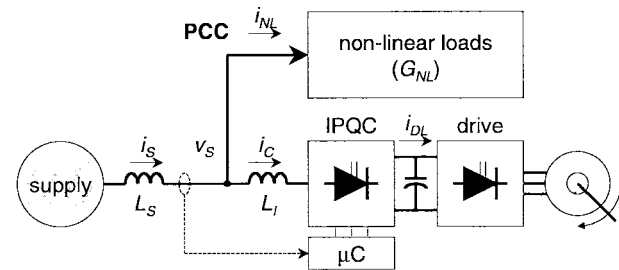


Fig. 2. IPQC Strategy.

A conventional active power quality compensation strategy is illustrated in Fig. 1 [1], [2]. The active power filter (APF) may operate directly off-line or isolated using an injection transformer. This strategy requires an additional inverter and controller functioning as an APF and the measurement of both the nonlinear load current (i_{NL}) and the compensating current (i_C).

The APF uses the measured nonlinear load current (i_{NL}) to compute current references for the compensating current (i_C) by using a power theory [4], [6]. The compensating current is regulated by an inner-loop current regulator.

The proposed three-phase integrated active rectifier and shunt power quality compensator (IPQC) is illustrated in Fig. 2. In this strategy, the IPQC functions as the active rectifier for one of the motor drives while performing power quality compensation for multiple nonlinear loads at the point of common coupling (PCC) and requires measurement of only the supply current (i_S).

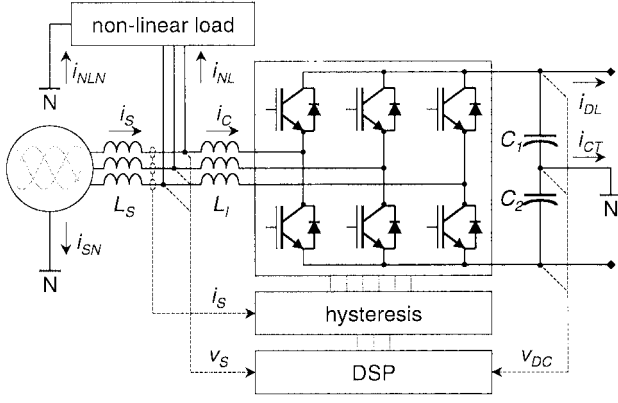


Fig. 3. IPQC topology.

The IPQC performs the following functions:

- improvement of the supply current (i_S) harmonic content in the presence of multiple nonlinear loads;
- improvement of the displacement power factor in the presence of multiple loads with a leading or lagging power factor;
- improvement of the supply current (i_{Sa}, i_{Sb}, i_{Sc}) balance;
- four-quadrant active rectifier operation.

II. PROPOSED IPQC TOPOLOGY

A shunt power quality compensator/APF requiring the measurement of only the supply current is proposed. The proposed three-phase four-wire topology is shown in Fig. 3; the topology differs from an active rectifier only by the position of current measurement. The four-wire topology decouples the IPQC phases, resulting in improved performance when using a simple per-phase current regulator [6].

The proposed strategy feeds the measured supply current (i_S) directly to a current regulator. The current regulator is supplied with a sinusoidal current reference (i_S^*) synchronized with the supply voltage. This current reference (i_S^*) corresponds to the ideal compensated supply current. The compensation current (i_C) is generated naturally by the current regulator feedback loop. The nonlinear load current (i_{NL}) is not directly measured, but the active components of the nonlinear load current (i_{NL}^A) and the dc-bus load (drive) current (i_{DL}) is estimated by the dc-bus voltage regulator. The resulting compensating current (i_C) may be determined by considering the summation of currents at the PCC

$$i_C(t) = i_S(t) - i_{NL}(t). \quad (1)$$

The use of an instantaneous current regulator (e.g., hysteresis) results in a fast response to supply current waveform distortion.

III. NEW SIMPLIFIED CONTROL ALGORITHM

A. Method of Operation

The control algorithm is responsible for the synthesis of a sinusoidal supply current reference (i_S^*) with the appropriate phase and amplitude while regulating the IPQC dc-bus voltage (V_{DC}).

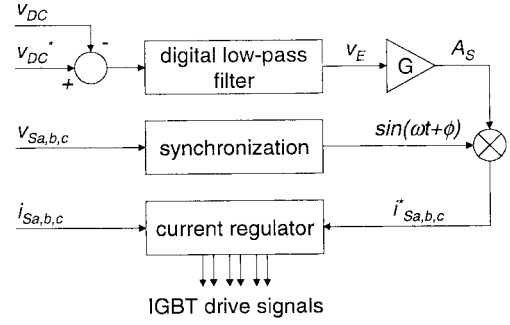


Fig. 4. Simplified IPQC control diagram.

The operation is explained by considering the active components of the supply (i_S^A), nonlinear load (i_{NL}^A), and compensating currents (i_C^A) [5, pp. 596–599, 625–627, 700–702], where

$$\begin{aligned} i_{NL}^A(t) &= G_{NL}v_S(t) \\ i_C^A(t) &= G_Cv_S(t) \\ i_S^A(t) &= G_Tv_S(t). \end{aligned} \quad (2)$$

The relation of the current active components is found by considering the summation of currents at the PCC,

$$i_S^A(t) = i_C^A(t) + i_{NL}^A(t). \quad (3)$$

The active component of the compensating current (i_C^A) is responsible for the charging and discharging of the IPQC dc bus and is a function of the active components of the supply (i_S^A) and nonlinear load current (i_{NL}^A). The active component of the compensating current (i_C^A) has to be controlled to regulate the dc-bus voltage (V_{DC}). The active component of the compensating current (i_C^A) is controlled by controlling the active component of the supply current (i_S^A), according to (3).

The active component of the nonlinear load current (i_{NL}^A) is estimated by the dc-bus voltage regulator. The dc-bus voltage (V_{DC}) is controlled by a load-conductance-based regulator [4], where the load consists of the active component of the nonlinear load current (i_{NL}^A) and the dc-bus (drive) load when the device is used as an active rectifier. The control algorithm is illustrated in Fig. 4. The dc-bus voltage regulator returns the supply current reference (i_S^*) and is implemented according to

$$\begin{aligned} v_E(t) &= \sum_{i=0}^{N-1} k_i(v_{DC}^* - v_{DC}) \cdot \delta(t - \Delta t \cdot i) \\ A_S &= \begin{cases} -A_{S(\text{MAX})}, & \text{if } G \cdot v_E(t) \leq -A_{S(\text{MAX})} \\ G \cdot v_E(t), & \text{if } -A_{S(\text{MAX})} \leq G \cdot v_E(t) \leq A_{S(\text{MAX})} \\ A_{S(\text{MAX})}, & \text{if } G \cdot v_E(t) \geq A_{S(\text{MAX})} \end{cases} \end{aligned} \quad (4)$$

$$\begin{aligned} i_{Sa}^*(t) &= A_S \sin(\omega t + \phi) \\ i_{Sb}^*(t) &= A_S \sin\left(\omega t + \phi + \frac{2}{3}\pi\right) \\ i_{Sc}^*(t) &= A_S \sin\left(\omega t + \phi - \frac{2}{3}\pi\right) \end{aligned} \quad (5)$$

where A_S is the amplitude of the supply current reference, and $A_{S(\text{MAX})}$ is the maximum allowed amplitude of the supply current. k_i are digital low-pass filter coefficients, Δt is the sampling period, and ω , ϕ the supply frequency and phase. G is a conductance associated with the dc-bus voltage error designed with the digital low-pass filter to satisfy the dynamic and steady-state dc-bus voltage regulation requirements. This conductance is related to G_T as defined in (2).

The dc-bus regulator provides a simple and efficient method of regulation, while the injection of undesired harmonics in the supply current (i_S) during transients may be reduced by proper selection of the low-pass filter time constant [3], [4].

The dc-bus capacitor voltages (V_{C1}, V_{C2}) are balanced by controlling the dc component of the center-tap current (i_{CT}) as defined in Fig. 3. The capacitor unbalance is related to the center-tap current by

$$(V_{C1} - V_{C2}) = \frac{1}{C} \int i_{CT} dt \quad (6)$$

where C is the total dc-bus capacitance.

The dc component of the center-tap current is controlled by adding a dc offset to the supply current references. A load-conductance-based regulator, similar to the dc-bus voltage regulator, is used for the capacitor voltage balancing.

B. Implementation

The experimental setup consists of a three-phase four-wire insulated gate bipolar transistor (IGBT) IPQC controlled by a low-cost fixed-point digital-signal-processor (DSP) (TMS320C50)-based controller. Current regulation is performed by fixed-band hysteresis.

A block diagram of the IPQC is shown in Fig. 3. The dc-bus voltage regulation, synchronization, as well as the current reference computation is implemented using the DSP. The DSP supplies the calculated supply current reference (i_S^*) to the current regulator.

Effective synchronization with the supply voltage (v_S) is required. This is achieved by using a correlation technique. This technique improves immunity to noise and waveform distortion, while providing feedback about the accuracy of the current state of synchronization. The N -point cross correlation given in (7) is used during synchronization

$$r_{xy}(l) = \sum_{n=0}^{N-1} x(n+l)y(n) \quad (7)$$

where $x(n)$ is the synchronized unity sinusoidal references and $y(n)$ is the measured supply voltage (v_S). N is such that $y(n)$ contains one period of the supply voltage (v_S). The correlation technique of synchronization evaluates (7) for three values of l ,

$$l = \left\{ 0, \quad +\frac{N}{4}, \quad -\frac{N}{4} \right\}.$$

The value of (7) is maximized for $l = 0$. By considering relative magnitudes of (7) evaluated for $l = \frac{N}{4}$ and $l = -\frac{N}{4}$, the polarity of the phase error (leading or lagging) of the unity sinusoidal reference with respect to measured supply voltage (v_S) is obtained. The unity sinusoidal reference is

TABLE I
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value	Unit
V_S	190	Vrms
V_{DC}	400	V
L_S	180	μH
L_f	2.2	mH
$N_1:N_2$	1.7:1	
C_1, C_2	9.9	mF

adjusted to correct the phase error. The value of (7) for $l = 0$ is used as feedback of the accuracy of the current state of synchronization, enabling efficient protection against inaccurate synchronization.

C. Control and Protection Issues

Efficient synchronization with the supply voltage (v_S) and the ability to detect an unsynchronized state is important, since the compensating current (i_C) is not measured. The power rating of the compensator is lower than the power rating of the total load. If accurate synchronization with the supply voltage is not maintained, the device may trip due to excessive reactive power being supplied. This prompted the use of the described correlation technique for synchronization.

If a supply line fault occurs and one or more of the supply phases enters a high-impedance state, current feedback for the corresponding phase is lost. Line-fault conditions are detected and the switching for the corresponding phase disabled. On-state voltage sensing for the switching devices is an effective method of protection during line-fault conditions and is implemented in most IGBT's and/or drivers.

If the required supply current exceeds the maximum allowed value, active power is drawn from the IPQC dc bus. This results in the discharging of the dc bus and may result in inverter overcurrent. The accuracy of the supply current (i_S) measurement cannot be guaranteed as result of measurement saturation and the IPQC is disabled for the duration of supply overcurrent. Careful consideration should be given to the sizing of the dc-bus capacitance.

IV. EXPERIMENTAL RESULTS

The topology shown in Fig. 3 was used for the experimental verification of the IPQC. The IPQC was connected to the PCC by an injection transformer with a turns ratio of $N_1 : N_2$. The parameters of the experimental setup are shown in Table I. A standard voltage-source inverter was used as the power stage and a TMS320C50 DSP-based controller was used to implement the protection and functions.

A. Harmonic Filtering

The harmonic filtering performance of the IPQC was tested with a six-pulse rectifier load. The measured results are shown in Fig. 5. Fig. 5(a) shows the compensated supply current (i_S), Fig. 5(b) the uncompensated supply current (i_S), Fig. 5(c) the normalized spectrum of the compensated supply current,

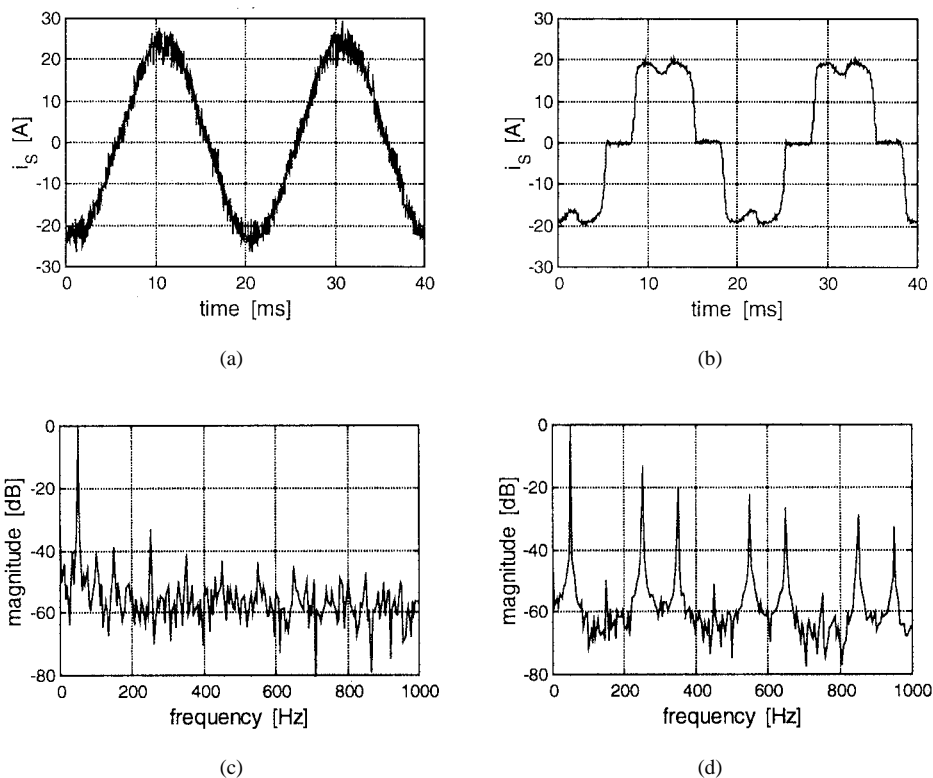


Fig. 5. Harmonic filtering performance.

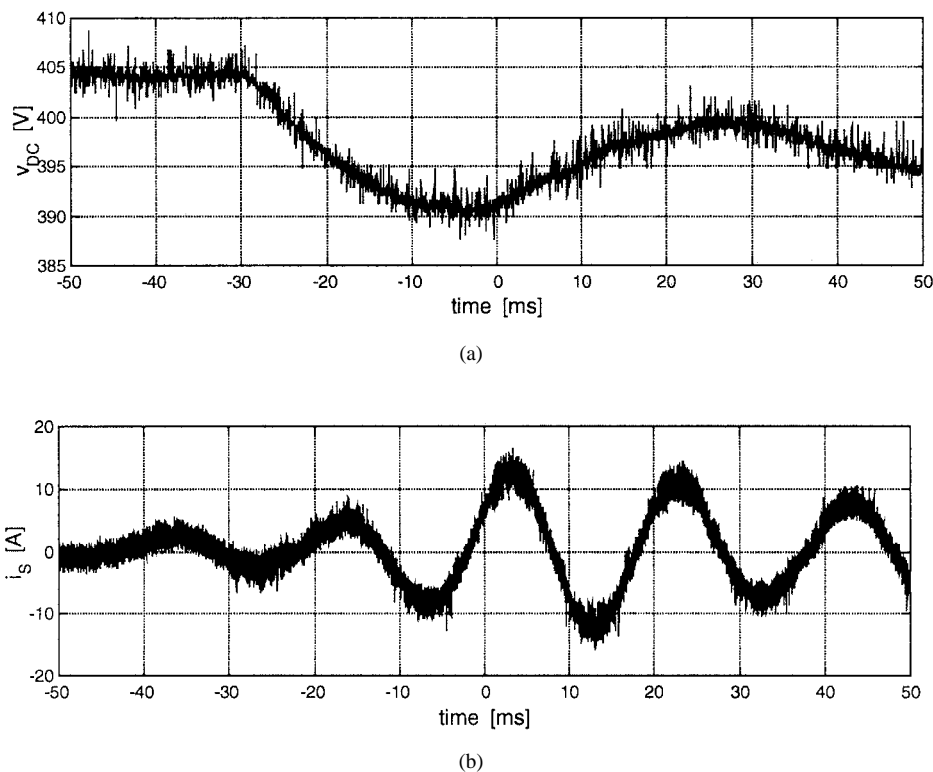


Fig. 6. Nonlinear load step response.

and Fig. 5(d) the normalized spectrum of the uncompensated supply current. The measured currents are in phase with the supply voltage as shown in Fig. 7.

The measured dc-bus voltage and supply current (i_s) for a 100% step in the nonlinear load current (i_{NL}) is shown

in Fig. 6. During nonlinear load transients, energy is supplied or absorbed by the IPQC dc-bus capacitor, resulting in reduced supply current harmonics. The improvement in the harmonic contents of the supply current is summarized in Table II.

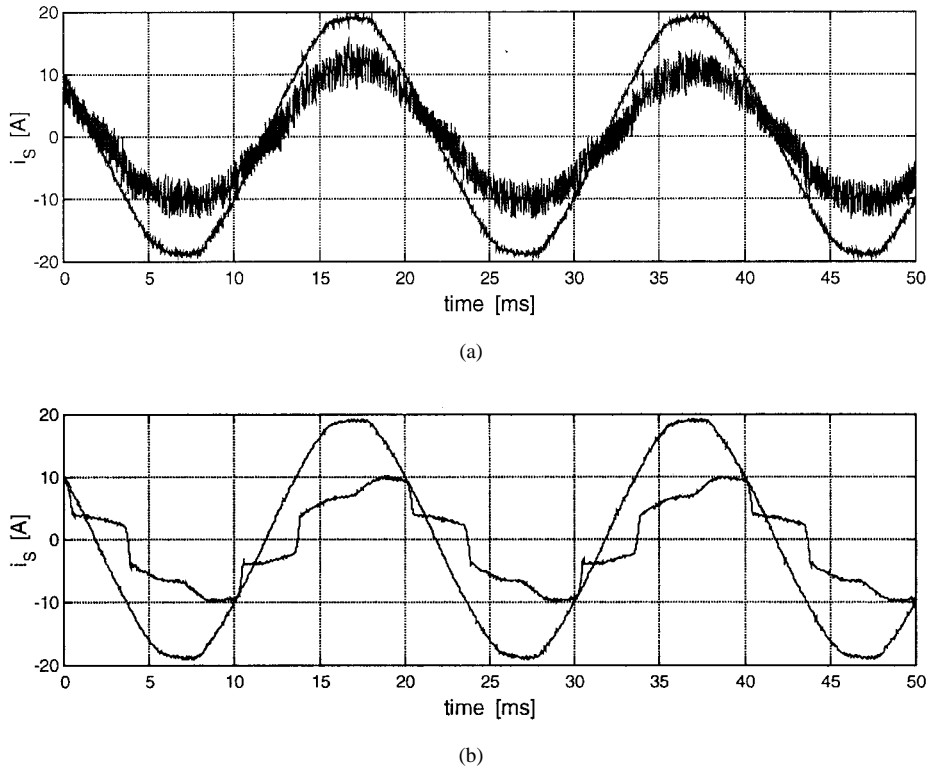


Fig. 7. Harmonic filtering and power factor correction.

TABLE II
HARMONIC FILTERING PERFORMANCE

Harmonic	Uncompensated (dB)	Compensated (dB)	Improvement (dB)
5	-13	-33.3	20.3
7	-20	-41.1	21.1
11	-22.5	-43.8	21.3
13	-26.7	-45.1	18.4
17	-28.9	-47.2	18.3
19	-32.7	-50.1	17.4

Variation in the dc-bus voltage is an accurate measure of the instantaneous active energy absorbed or supplied by the IPQC. The dynamic capability of the IPQC is determined by the dynamic response of the dc-bus voltage regulator and size of the dc-bus storage elements. A dc-bus voltage regulator with a high bandwidth could adversely affect harmonic filtering, while a regulator with a too low bandwidth may prove inadequate during load transients. The size of the dc-bus energy storage and expected load requirements should be considered during the design of the dc-bus voltage regulator.

B. Power-Factor Correction

The ability of the device to improve the displacement power factor, while simultaneously performing harmonic filtering, was tested by compensating for a six-pulse rectifier load in parallel with an inductive load. The measured results are shown in Fig. 7. Fig. 7(a) shows the compensated supply current (i_s), and Fig. 7(b) shows the uncompensated supply current (i_s).

C. Active Rectifier Operation

The ability of the device to regulate the dc-bus voltage, while operating as an active rectifier, was tested by applying a -7 A (-2.8 kW) and $+8$ A ($+3.2$ kW) dc-bus (drive) load step (i_{DL}). The measured results are shown in Fig. 8. Fig. 8(a) shows dc-bus voltage (v_{DC}) regeneration step response, Fig. 8(b) the dc-bus voltage (v_{DC}) load step response, Fig. 8(c) the supply current (i_s) regeneration step response, and Fig. 8(d) the supply current load step response (i_s). The load-conductance-based regulator results in a dc-bus voltage steady-state error while undesired injected supply current harmonics during load transients are reduced by proper selection of the load-pass filter time constant.

D. Load Unbalance

The performance of the device during load unbalance was tested by applying a load -step on one phase at 25 ms in Fig. 9. The measured step-response is shown in Fig. 9. Fig. 9(a) shows the compensated supply currents, and Fig. 9(b) shows the uncompensated supply currents.

The dc-bus center-tap current and the supply neutral current during load unbalance is shown in Fig. 10. Fig. 10(a) shows the dc-bus center-tap current (i_{CT}), and Fig. 10(b) shows the supply neutral current (i_{SN}).

E. Supply Unbalance

The performance of the device under supply unbalance was tested by disconnecting one of the supply phases. The measured results are shown in Fig. 11. Fig. 11(a) shows the

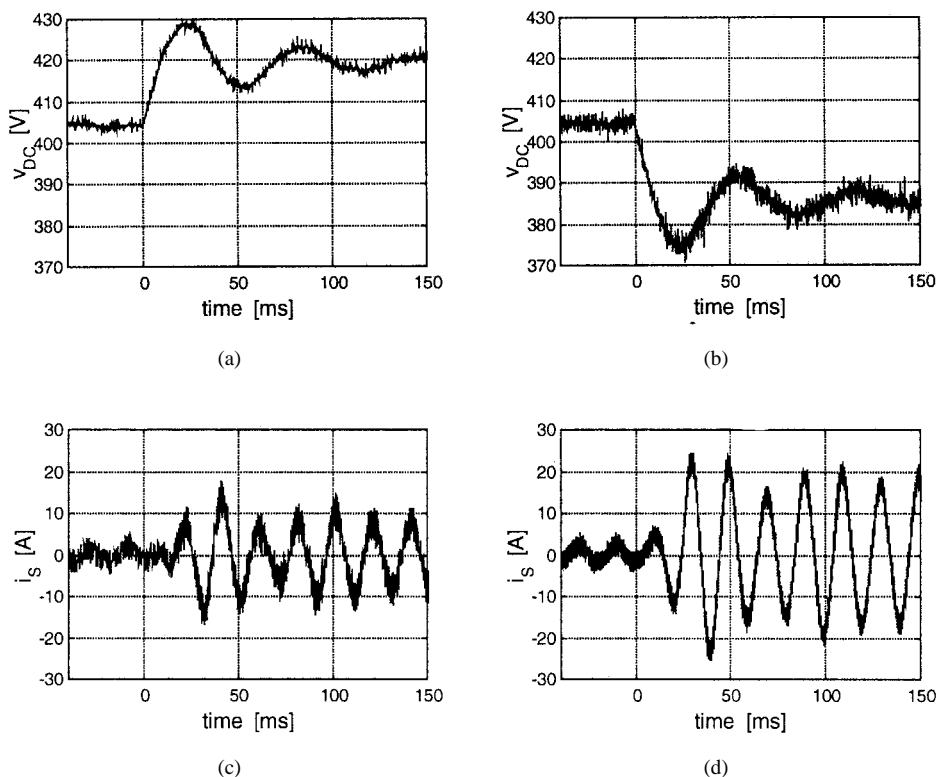


Fig. 8. DC-bus (drive) load step response.

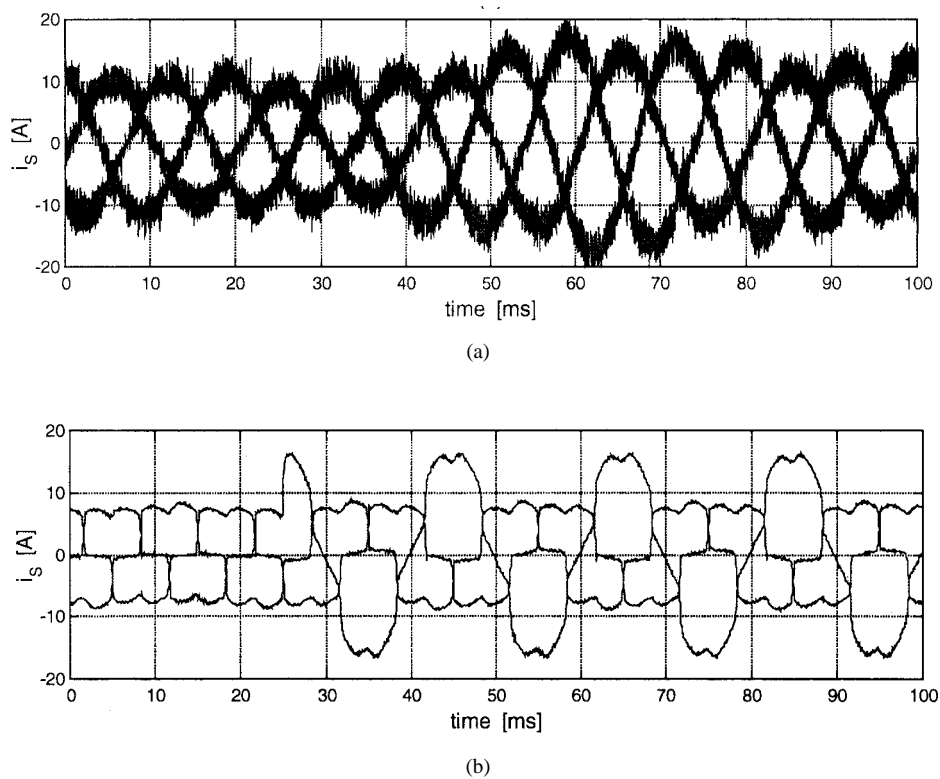


Fig. 9. Supply current balancing during load unbalance.

compensated supply current (i_S), Fig. 11(b) the uncompensated supply current (i_S), Fig. 11(c) the supply neutral current during compensation (i_{SN}), and Fig. 11(d) the normal supply neutral current (i_{SN}).

V. CONCLUSIONS AND RECOMMENDATIONS

An IPQC was developed and tested. The proposed IPQC requires the measurement of only three supply currents and can function as an active rectifier, while improving the supply

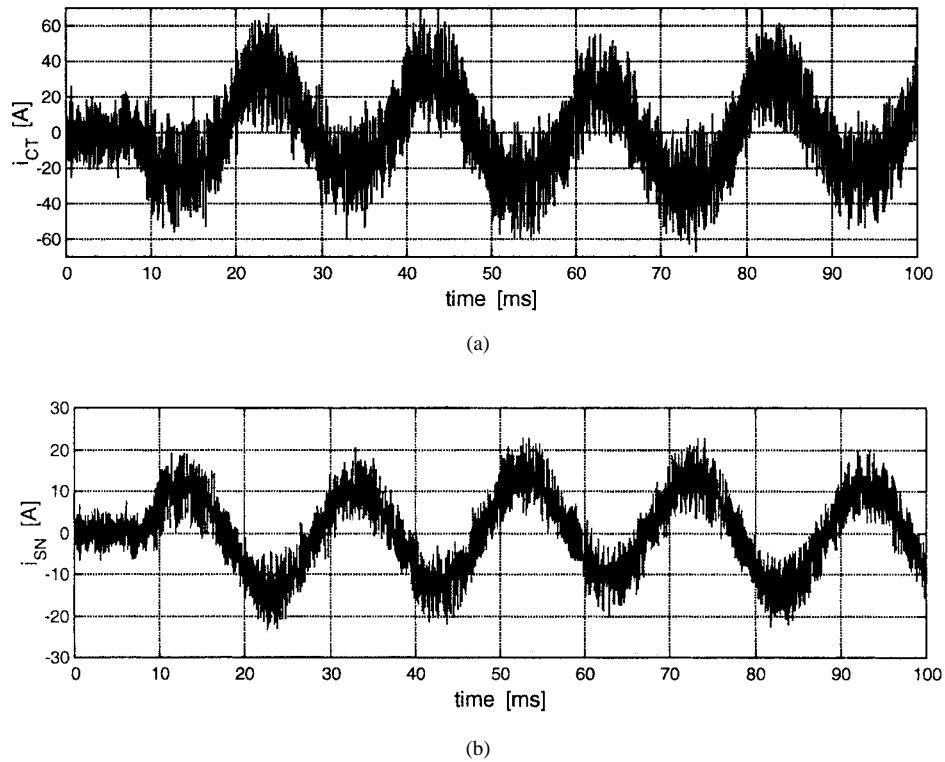


Fig. 10. Supply neutral and dc-bus center-tap currents during load unbalance.

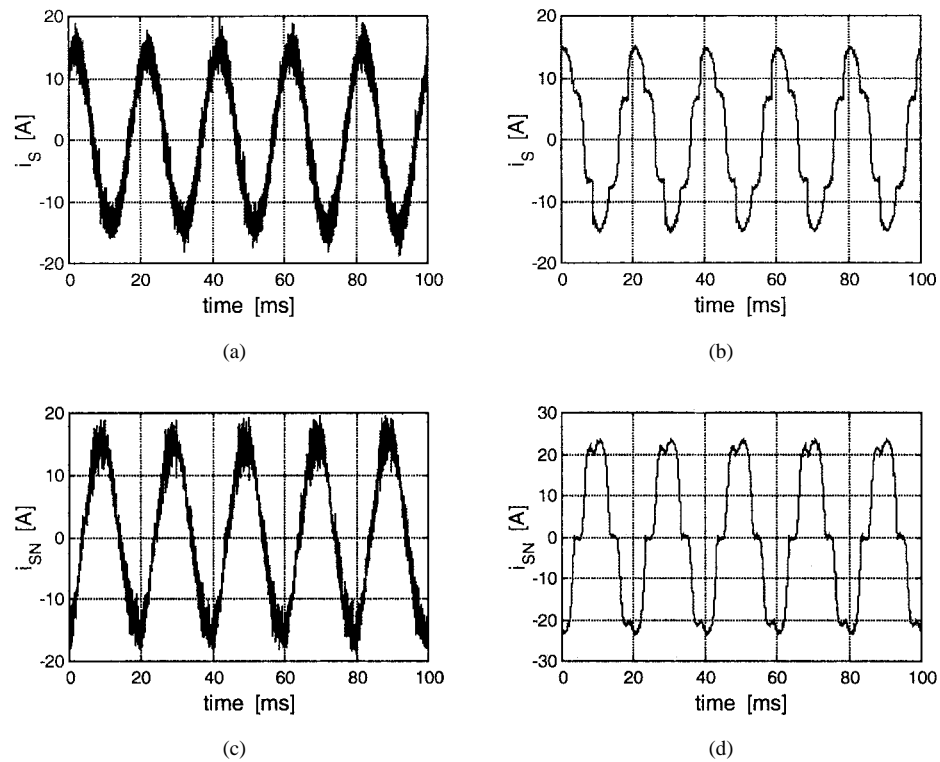


Fig. 11. Supply line and neutral current during supply unbalance.

power factor and harmonic contents for multiple nonlinear loads.

In plants containing multiple nonlinear loads, the IPQC may be installed as an active rectifier for one of the (drive) loads.

The device will then compensate for harmonics generated by all the nonlinear loads at the PCC.

In plants containing one or more active rectifiers (with supply current feedback), one of the active rectifiers can be

TABLE III
APF-IPQC COMPARISON

Conventional APF	IPQC
A dedicated power stage and controller functioning as an APF is required.	The power stage and controller performs power quality compensation while functioning as a regulated dc voltage source.
The measurement of the converter currents and load currents is required.	The measurement of only the supply currents is required.
The implementation of hardware protection is simple.	The implementation of hardware protection is more complex.

modified to operate as an IPQC to compensate for other non-linear loads with minimal changes in hardware and controller software.

The IPQC performs the following functions:

- improvement of the supply current (i_S) harmonic content in the presence of multiple nonlinear loads;
- improvement of the displacement power factor in the presence of multiple loads with a leading or lagging power factor;
- improvement of the supply current (i_{Sa}, i_{Sb}, i_{Sc}) balance;
- four-quadrant active rectifier operation.

A comparison of the IPQC to a conventional APF is summarized in Table III.

REFERENCES

- [1] L. Gyugi and E. C. Strycula, "Active AC power filters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1976, p. 529.
- [2] H. Akagi, "New trends in active filters for power conditioning," *IEEE Trans. Ind. Applicat.*, vol. 32, pp. 1312–1322, Nov./Dec. 1996.
- [3] S. Bhowmik, R. Spée, G.C. Alexander, and J. H. R. Enslin, "New simplified control algorithm for synchronous rectifiers," in *Proc. IEEE IECON'95*, 1995, pp. 494–499.
- [4] J. H. R. Enslin and J. D. van Wyk, "A new control philosophy for power electronic converters as fictitious power compensators," *IEEE Trans. Power Electron.*, vol. 5, pp. 88–97, Jan. 1990
- [5] Fryze, "Wirk-, Blind-, und Scheinleistung in Elektrischen Stromkreisen mit nichtsinusiodalförmigem Verlauf von Strom und Spannung," *ETZ*, vol. 53, no. 25, 1932.
- [6] G. Dinkel and R. Gretsche, "Kompensator für Oberschwingungen und Blindleistung," *ETZ Arch.*, vol. 9, no. 1, pp. 9–14, 1987.



A. D. le Roux received the B.Eng. and M.Eng. degrees from the University of Stellenbosch, Stellenbosch, South Africa, where he is currently working towards the Ph.D. degree in power electronics.

His fields of interest include power quality, electrical drives and high-performance digital controllers and current regulators.



J. A. du Toit received the B.Eng. and M.Eng. degrees from the University of Stellenbosch, Stellenbosch, South Africa, where he is currently working towards the Ph.D. degree in power electronics.

His fields of interest include high-performance digital controllers, distributed control of power electronics, and control of multilevel and stacked converter topologies.



J. H. R. Enslin (M'85–SM'92) was born in Bloemfontein, South Africa, in 1959. He received the B.Eng., M.Eng., and D.Eng. degrees in electrical and electronics engineering from Rand Afrikaans University, Johannesburg, South Africa, in 1981, 1983, and 1988, respectively.

During 1982 and 1983, he was with the Department of Electrical and Electronics Engineering, Rand Afrikaans University. He joined the Department of Electrical Engineering, University of Pretoria, Pretoria, South Africa, in 1986, after some industrial experience with the South African Railways and Signal Corps. Since 1991, he has been a Professor in the area of power systems at the University of Stellenbosch, Stellenbosch, South Africa. He is currently also the Technical Manager (Distribution) of the South African Power Systems Studies Institute, a joint project between ESKOM and the Electric Power Research Institute. He is involved in research, consulting, and industrial work in several fields of power systems and power electronics, including FACTS, custom power, power quality, renewable energy and electrical drives. He has authored or coauthored more than 150 papers in international technical journals, six of which have won prize paper awards, and is the holder of seven international patents.

Dr. Enslin is a Registered Professional Engineer with the South African Council of Professional Engineers and a senior member of the South African Institute of Electrical Engineers. He is also a member of the CIGRE Active Filter Group.