An Implementation of an Adaptive Control Algorithm for a Three-Phase Shunt Active Filter

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***Abstract*—This paper deals with the hardware implementation of a shunt active filter (SAF) for compensation of reactive power, unbalanced loading, and harmonic currents. SAF is controlled using an adaptive-linear-element (Adaline)-based current estimator to maintain sinusoidal and unity-power-factor source currents. Three-phase load currents are sensed, and using least mean square (LMS) algorithm-based Adaline, online calculation of weights is performed and these weights are multiplied by the unit vector templates, which give the fundamental-frequency real component of load currents. The dc bus voltage of voltage source converter (VSC) working as a SAF is maintained at constant value using a proportional–integral controller. The switching of VSC is performed using hysteresis-based pulsewidth-modulation indirect-current-control scheme, which controls the source currents to follow the derived reference source currents. The practical implementation of the SAF is realized using dSPACE DS1104 R&D controller having TMS320F240 as a slave DSP. The MATLAB-based simulation results and implementation results are presented to demonstrate the effectiveness of the SAF with Adaline-based control for load compensation.**

***Index Terms*—Adaptive linear element (Adaline), harmonics, reactive power, shunt active filter (SAF), unbalance.**

I. Introduction

THE PROBLEM of reactive power burden has been a concern for power engineers for many years. This problem is aggravated in harmonic environment caused by power electronic converters. This nonlinear current having a high amount of harmonics distorts the ac voltage at the point of common coupling (PCC) and therefore affects the other neighboring loads connected to the same system [1], [2]. Excessive reactive power demand increases feeder losses and reduces the active power flow capability of distribution system, whereas unbalancing affects the operation of transformers and generators. The advent of custom power device technology has proved to be a boon for the electric distribution system facing these problems (reactive power burden, harmonics, and unbalanced loading). The custom power device such as shunt active filter (SAF) is found to be quite suitable to cater to the aforesaid problems [3]. The major issue related to the effective operation of SAF is its controllability to compensate reactive power, harmonics, and unbalanced loading.

The control of SAF depends on two major factors: the first is extraction of reference currents, and second is the method of generation of pulsewidth-modulation (PWM) signals using these extracted reference currents. The techniques reported in the literature for reference current extraction are instantaneous reactive power theory, instantaneous symmetrical components, scheme based on neural network, rotating reference frame, and per phase computation [4]–[8]. Instantaneous reactive power theory works on the computations of active and reactive powers through three-phase to two-phase transformation and fails to work properly under a distorted voltage condition [4]. The SRF theory is based on the filtering of dc components of currents by a low-pass filter (LPF) in synchronously rotating frame [5]. Reported neural-network-based schemes require offline training for a set of loads which makes the scheme suitable only for particular loads [7], [8]. Moreover, after the extraction of reference currents, the important aspect is whether the control should be provided on SAF currents (direct current control) or on source currents (indirect current control) [9], [10]. The indirect current control provides an advantage over the direct current control as it has instantaneous compensation and suppresses the switching frequency noise. Some of the researchers have proposed Adaline-based approach to estimate reactive power and harmonic content in the current [11], whereas Abdeslam *et al.* [12] use complex combination of Adalines to provide compensation for reactive power and harmonics, but it does not include unbalance compensation and self-supporting dc bus feature of SAF.

This paper deals with the control of SAF with self-supporting dc bus and compensation of reactive power, harmonics, and unbalanced loading. The extraction of reference source currents is carried out using least mean square (LMS) algorithm-based Adaline, which is a simple and fast method of current extraction [13]. Only three Adalines are used to extract the three-phase positive-sequence fundamental-frequency real component of load currents. The LMS algorithm [14], [15], with the online calculation of weights, responds well for severe load changes. The dc bus voltage of the voltage source converter (VSC) of SAF is self-supported using a proportional–integral (PI) controller, which computes the loss component of the current in SAF. The proposed method, together with indirect current control, improves the effectiveness of the SAF for compensation of load currents. The proposed control scheme can easily be implemented on digital processors and employs the least calculations. In-phase unit templates of the synchronized signals are generated by filtering voltage signals using a

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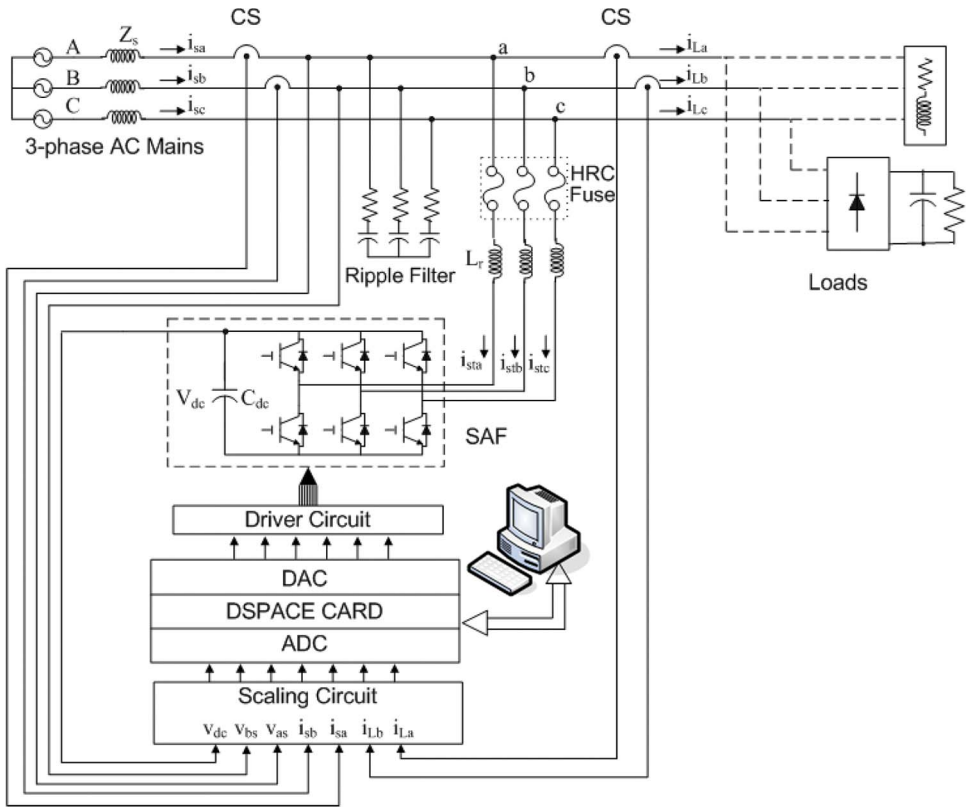


Fig. 1. Block diagram of the power and control circuit of SAF.

second-order digital filter. The distortion in the voltage is filtered, and a reference signal is obtained without delay by filtering the sequence component ahead of the present signal. This scheme is simulated under the MATLAB environment using SIMULINK and power system blockset toolboxes, and the results are verified by implementation of the control scheme in real time using dSPACE DS1104 R&D controller. The performance of the proposed scheme is demonstrated through simulated and experimental results.

II. System Configuration and Hardware Description

The implementation of a SAF for reactive power compensation, unbalance compensation, and harmonic mitigation requires a thoughtful selection and design of components such as VSC, dc bus capacitor, ac inductors, and interfacing hardware circuits. Another important factor that affects the performance of the SAF is the selection of a processor, which should be fast enough to provide compensation for higher order harmonics. Apart from the speed of the processor, the speed of interfacing circuits and sensors also affects the performance of the SAF. Protection circuit is used to safeguard the system from any malfunction.

Fig. 1 shows the detailed block diagram of the SAF system. This figure shows the three-phase ac mains system feeding linear and nonlinear loads. The protection is provided to the circuit using fast HRC fuses and master circuit breakers.

The control of SAF system is achieved through the Adaline-based algorithm implemented using dSPACE. The load currents of phases-a and -b (i_{La} and i_{Lb}) are sensed using Hall effect current sensors (LEM CT-100S). Since the implementation is carried out for a three-phase three-wire system, a three-phase current is calculated by assuming that the sum of three currents is zero. Similarly, another set of current sensors is used to sense source currents of phases-a and -b (i_{sa} and i_{sb}). Three voltage sensors (LEM CV3-1500) are used to sense phase-a, phase-b, and dc-link voltages. The signals taken from the sensors are fed to the scaling circuits consisting of fast operational amplifiers (OP-07). The outputs of the scaling circuits are given to analog-to-digital converters (ADCs) of the dSPACE. The software implementation of control algorithm is realized in MATLAB blocks in DSP dSPACE to generate the switching signals for insulated-gate bipolar transistors (IGBTs) of SAF using Adaline-based reference current extraction technique and hysteresis PWM current controller. These switching signals are fed to SKHI 22B drivers, which finally provide the gate signals for the IGBT modules (SKM 100GB128DN) used to realize SAF.

The signals sampled at ADC are first given appropriate gains (as per the conversion factor of sensing and scaling circuit) to get the sensed signal value. For generation of unit vector templates, the sampled phase voltage is filtered by a second-order Chebyshev filter (filter parameters are provided in Table I). The phase-c voltage is constructed using phase-a and phase-b voltages. The bandpass filter introduces some delay in the signal, this delay is measured in real time, and phase-a is further appropriately delayed in processor to construct phase-b signal. Similarly, phases-c and -a filtered signals are also generated. Three voltages are transformed to two-phase signals, and the amplitude is calculated by square root of the sum of squared two-phase signals. This amplitude is used to divide the

TABLE I
SYSTEM PARAMETERS

Load	Three 3-Φ Diode bridge converter with LC filter at dc side with L=1.4mH and C=500μF
Non-linear load	Resistor at dc side of diode bridge converter, R_{dc}=20 Ω
Non-linear & unbalanced load	Resistor at dc side of diode bridge converter, R_{dc}=47.5 Ω Resistor connected between a & b phase R_{ab}=26.8 Ω
VSC	DC link capacitor C_{dc}=1650μF, AC inductor=2.5mH, Ripple Filter: C=10μF and R=25Ω, f_s=12.5kHz.
Chchebyshev filter	feed-forward coefficients; 0.4725e-3, 0.945e-3, 0.4725e-3 feed-backward coefficients; 1, 1.947, 0.9489 Bandwidth; 100Hz
PI Controller	K_{pdc}=0.3, K_{Idc}=1.0

three-phase voltages to get unit templates. The Adaline-based extraction scheme is used for extraction of real fundamental-frequency component of the load current. For self-support of the dc bus voltage of SAF, a PI controller is used which compares sensed dc bus voltage with its reference value. The output of PI controller is added to equivalent average weight estimated by Adaline. The basic building block of the scheme and its mathematical equations are discussed in the next section. For implementation, the control algorithm is run at a fixed step size of 78.125 μs, and therefore, the maximum switching frequency of VSC of SAF is fixed at 12.8 kHz.

III. CONTROL ALGORITHM

The operation of the SAF system requires ac mains to supply real power needed to the load and some losses (switching losses of devices, losses in the reactor, and dielectric losses of dc capacitor) in the SAF. Therefore, the reference source currents that are used to decide the switching of the SAF have two parts: one is the real fundamental-frequency component of the load current, which is being extracted using Adaline, and another component, which corresponds to the losses in the SAF, is estimated using a PI controller over the dc voltage of SAF. The output of the PI controller is added to the weight calculated by the Adaline to maintain the dc bus voltage of the SAF. Fig. 2(a) shows the control algorithm of SAF for the compensation of reactive power, unbalanced loading, and harmonic load currents.

A. Extraction of Real Positive-Sequence Fundamental-Frequency Current From Load Current

The basic theory of the proposed decomposer is based on the LMS algorithm [14], [15] and its training through Adaline, which tracks the unit vector templates to maintain minimum error. The basic concept of theory used here can be understood by considering the analysis in a single-phase system, which is given hereinafter.

The load current, which consists of an active current (i_p^+), reactive current (i_q^+) for positive sequence, negative sequence current (i^-), and harmonic frequency current (i_h), can be decomposed in parts as

$$i_L = i_p^+ + i_q^+ + i^- + i_h. \tag{1}$$

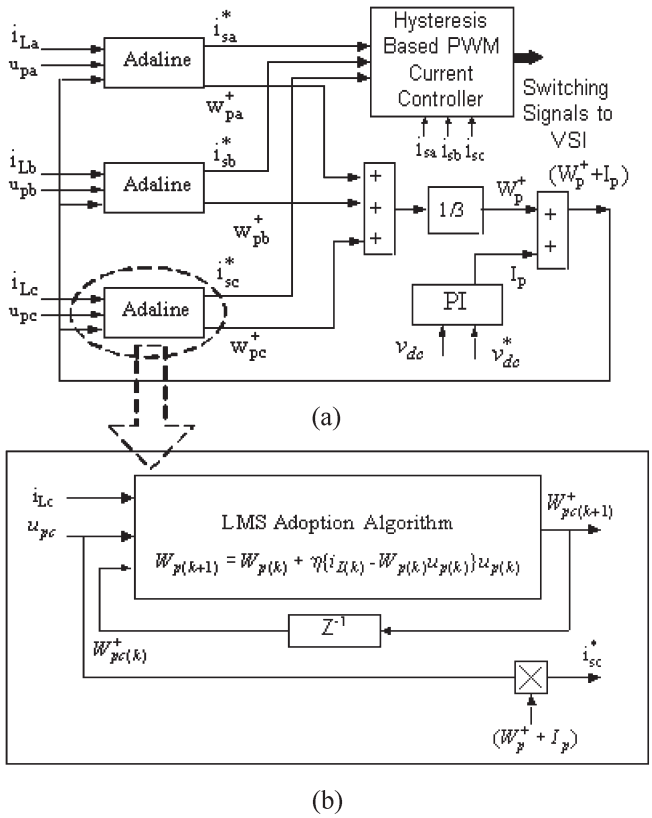


Fig. 2. (a) and (b) Control block diagram of the reference current extraction scheme.

The control algorithm is based on the extraction of current component in phase with the unit voltage template. To estimate the fundamental-frequency positive-sequence real component of the load current, the unit voltage template should be in phase with the system voltage and should have unit amplitude. The unit voltage template derived from the system phase voltage can be represented as

$$u_p = v_{\rm pcc}/V \tag{2}$$

where $v_{\rm pcc}$ is the filtered instantaneous voltage at the PCC and V is an amplitude of this voltage.

For proper estimation of current components of the load current, unit voltage template must be undistorted. For generation of unit vector templates, the sampled phase voltage is filtered by a second-order Chebyshev bandpass filter. The active power component of the load current for a single phase is computed by multiplying weight with the unit template, and this weight (W_p) is estimated using the Adaline technique. This weight is variable and changes as per the load current and magnitude of phase voltage. The scheme for computing weights corresponding to the fundamental-frequency real component of the load current (for three-phase system), based on the LMS-algorithm-tuned Adaline technique, tracks the unit vector template to maintain minimum error. The estimation of weight is given as per the following expression:

$$W_{p(k+1)} = W_{p(k)} + \eta \left\{ i_{L(k)} - W_{p(k)} u_{p(k)} \right\} u_{p(k)}. \tag{3}$$

The value of η (convergence coefficient) decides the rate of convergence and accuracy of estimation. The practical range of

convergence coefficient lies in between 0.01 and 1.0. The higher value of η increases the rate of convergence of weights but, at the same time, leads to inaccurate results, whereas the low value of η increases the accuracy of estimation but leads to slow convergence of weights. The best tradeoff is observed in accuracy and rate of convergence with η equal to 0.2. Three-phase currents corresponding to the positive-sequence real component of the load current may be computed by multiplying three-phase unit templates with equivalent average weight, which is given as

$$W_p^+ = \left(W_{\rm pa}^+ + W_{\rm pb}^+ + W_{\rm pc}^+\right)/3. \tag{4}$$

For proper estimation of reference currents, the weights are averaged to compute the equivalent weight for positive-sequence current component in the decomposed form. The averaging of weights helps in removing the unbalance in the current components.

B. PI Controller for Maintaining Constant DC Bus Voltage of SAF

To compute the second component of reference active current, a reference dc bus voltage is compared with the sensed dc bus voltage of SAF. The comparison of sensed dc bus voltage to the reference dc bus voltage of VSC of SAF results in a voltage error, which in the nth sampling instant is expressed as

$$v_{{\rm dcl}(n)} = v_{{\rm dc}(n)}^* - v_{{\rm dc}(n)}. \tag{5}$$

This error signal $v_{{\rm dcl}(n)}$ is processed in a PI controller, and output $\{I_{p(n)}\}$ at the nth sampling instant is expressed as

$$I_{p(n)} = I_{p(n-1)} + K_{\rm idc}\left\{v_{{\rm dcl}(n)} - v_{{\rm dcl}(n-1)}\right\} + K_{\rm pdc} v_{{\rm dcl}(n)} \tag{6}$$

where $K_{\rm pdc}$ and $K_{\rm idc}$ are the proportional and integral gains of the PI controller.

The output of the PI controller accounts for the losses in SAF, and it is considered as loss component of the current, which is added with the weight, estimated using the Adaline corresponding to the fundamental-frequency positive-sequence reference active load current component. Therefore, the total real reference current has a component corresponding to the load, and a component corresponding to feed the losses of SAF is expressed as

$$\begin{aligned} i_{\rm sa}^* &= \left(W_p^+ + I_p\right) u_{\rm pa} \\ i_{\rm sb}^* &= \left(W_p^+ + I_p\right) u_{\rm pb} \\ i_{\rm sc}^* &= \left(W_p^+ + I_p\right) u_{\rm pc}. \end{aligned} \tag{7}$$

These currents are considered reference source currents $i_{\rm ref}(i_{\rm sa}^*, i_{\rm sb}^*, i_{\rm sc}^*)$, and along with sensed source currents $i_{\rm act}(i_{\rm sa}, i_{\rm sb}, i_{\rm sc})$, these are fed to the hysteresis-based PWM current controller to control the source currents to follow these reference currents. The switching signals generated by the PWM current controller control sensed source currents close to these reference currents. This current control (indirect current control) results in control of the slow-varying source currents (as compared to SAF currents) and therefore requires less computational efforts [9]. Moreover, this scheme can instantaneously compensate the source currents (negligible effect of computational delay of processor), which is not possible with direct current control [10]. The switching signals are generated on the following logic.

1) If $(i_{\rm act}) > (i_{\rm ref} + hb)$, upper switch of the leg is ON and lower switch is OFF.
2) If $(i_{\rm act}) < (i_{\rm ref} - hb)$, upper switch of the leg is OFF and lower switch is ON.

Here, hb is the hysteresis band around the reference current $i_{\rm ref}$.

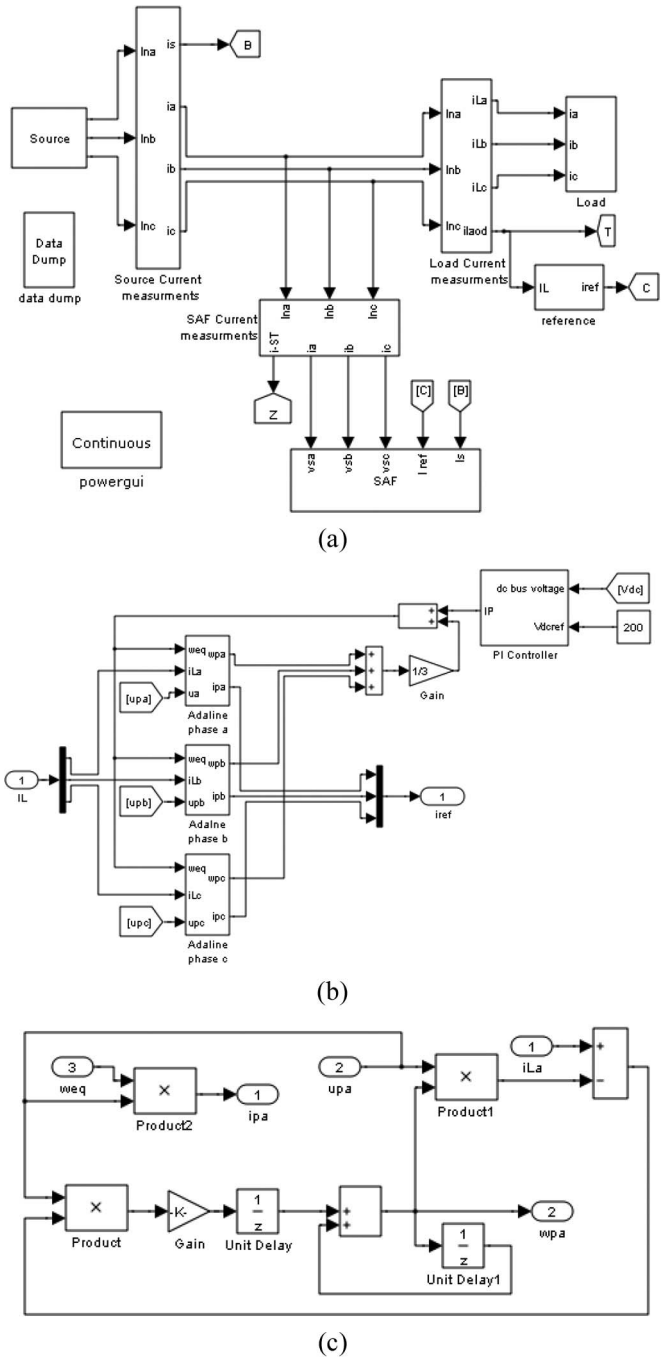


Fig. 3. (a) MATLAB-based model of the SAF system. (b) MATLAB-based block diagram for extraction of reference currents. (c) MATLAB-based block diagram for implementation of Adaline.

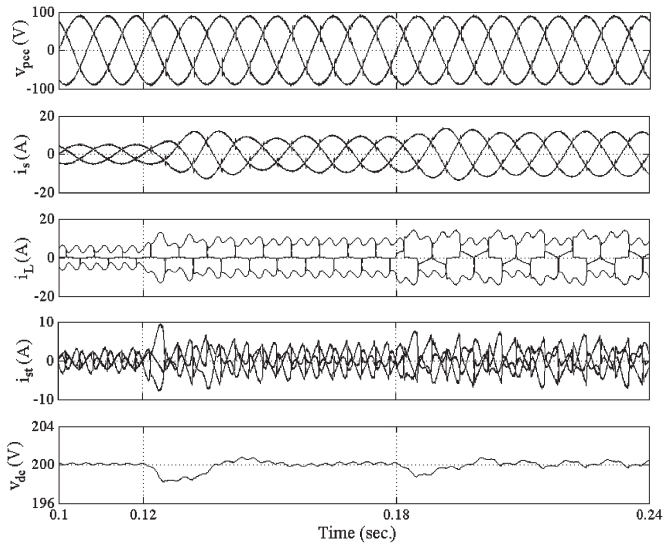


Fig. 4. Dynamic response of the SAF system.

The weights are computed online using the LMS algorithm. The update equation of weights based on the LMS algorithm is described in (3) for each phase. The structure of such Adaline control is shown in Fig. 2(b). Weights are averaged not only for averaging at fundamental frequency, but this cancels out the sinusoidally oscillating components in weights present due to harmonics in the load currents. The averaging of weights in different phases is shown in Fig. 2(a). Thus, Adaline is trained at fundamental frequency of a particular sequence in phase with voltage. Fig. 2(a) and (b) shows the detailed scheme implemented for control of SAF.

Because of the unbalance in load currents, the second harmonic ripple is produced in the dc bus voltage. This ripple has to be filtered out before feeding the signal to the PI controller; otherwise, this may cause the harmonics component in the source currents. For this purpose, the dc bus voltage is filtered using an LPF. Since the major amount of the reference current (load current component) is computed using Adaline-based extractor, the effect of the delay caused by the LPF is negligible in practical cases.

IV. MATLAB-Based Simulation of SAF

Fig. 3(a) shows the MATLAB model of the SAF system. The nonlinear load is modeled using a three-phase diode bridge converter connected to ac mains. At the dc bus of diode bridge converter, an inductor–capacitor filter combination is employed. The unbalanced load is realized through connecting a resistive load between phase-a and phase-b. The simulation is carried out in a continuous mode at $78.5 * 10^{-6}$ step size with ode15s(stiff/NDF) solver.

A detailed control scheme is shown in Fig. 3(b) and (c). Fig. 3(b) shows the control scheme with three Adaline blocks (each for one phase) and a PI controller to maintain the dc bus voltage of SAF. The flows of signals are such that the sensed load currents are fed to Adaline block which estimates the weight corresponding to the real fundamental-frequency part of the load currents. The loss part of the reference current is estimated using a PI controller. Fig. 3(c) shows the simulation model of Adaline for phase-a, which is a realization of Widrow Hoff's rule given in (3).

Fig. 4 shows the dynamic performance of the SAF system. The load on the SAF system is kept at 0.3 kW initially for time $t = 0.1-0.12$ s. The load compensation in terms of harmonic

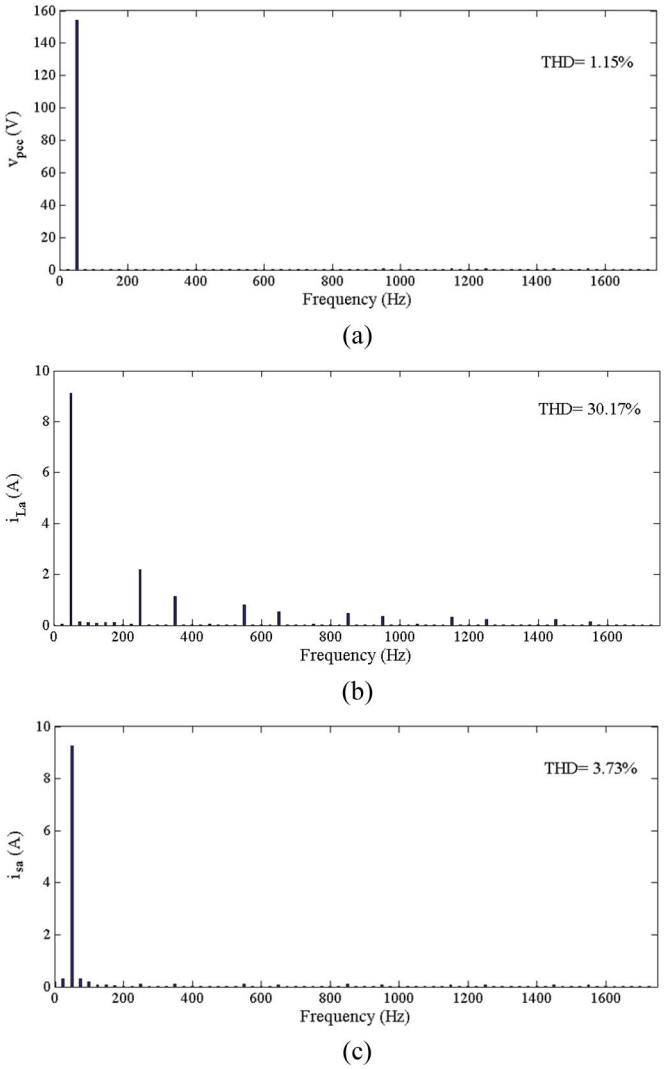


Fig. 5. Harmonic spectra of phase-a (a) voltage at PCC, (b) load current, and (c) source current.

TABLE II
RMS and %THD Values of Voltage at PCC, Load Current, and Source Current

		RMS values of voltage at PCC (V), load current and source current (A)			%THD of voltage at PCC, load current and source current		
		Ph-a	Ph-b	Ph-c	Ph-a	Ph-b	Ph-c
Light load	v_{pcc}	109.5	109.5	109.5	0.56	0.59	0.63
	i_L	3.6	3.6	3.6	35.67	35.34	35.25
	i_s	3.4	3.5	3.4	1.82	1.70	1.85
Peak load	v_{pcc}	109.4	109.4	109.4	1.15	1. 18	1.10
	i_L	6.7	6.7	6.7	30.17	30.46	30.10
	i_s	6.4	6.4	6.4	3.73	4.74	4.57
Unbalanced load	v_{pcc}	109.3	109.4	109.4	2.12	1.97	1.88
	i_L	8.4	8.4	6.7	23.87	23.47	30.43
	i_s	7.7	7.8	7.9	2.90	3.01	2.79

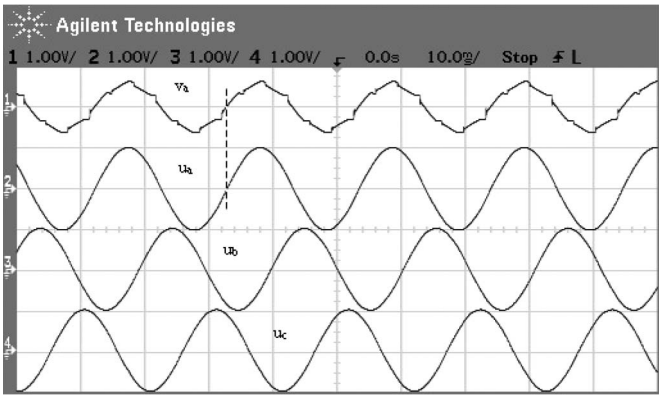


Fig. 6. Waveforms of unit voltage templates (scales: 150 V/div for channel 1 and 1 V/div for channels 2, 3, and 4).

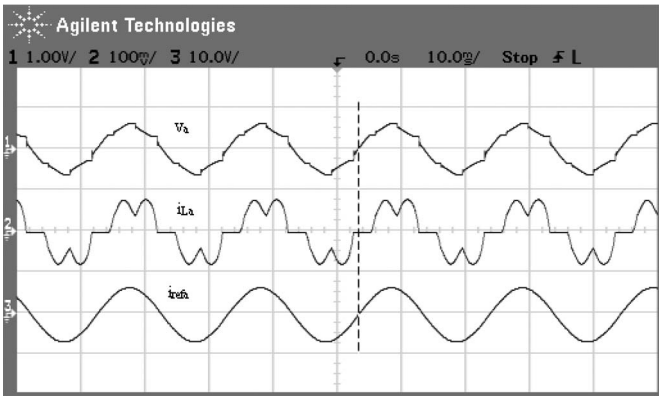


Fig. 7. Waveform of extracted phase-a reference current (scales: 150 V/div for channel 1 and 10 A/div for channels 2 and 3).

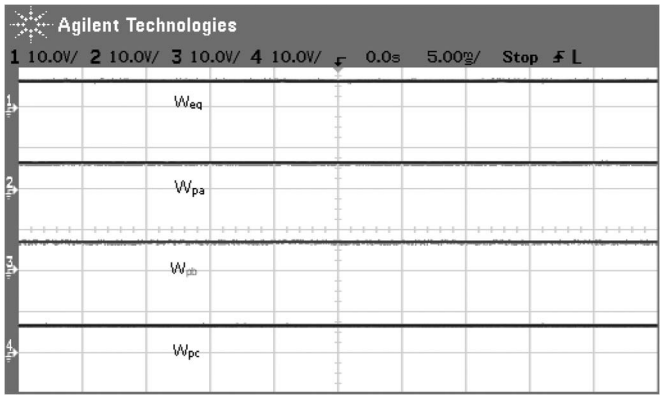


Fig. 8. Waveforms of equivalent weight with three-phase weights (scales: 10 units/div for channels 1, 2, 3, and 4).

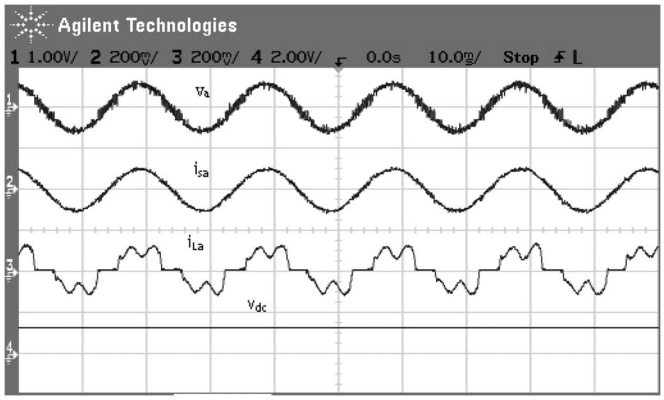


Fig. 9. Recorded steady-state waveform of compensation by SAF with nonlinear load (scales: 150 V/div for channel 1, 20 A/div for channels 2 and 3, and 300 V/div for channel 4).

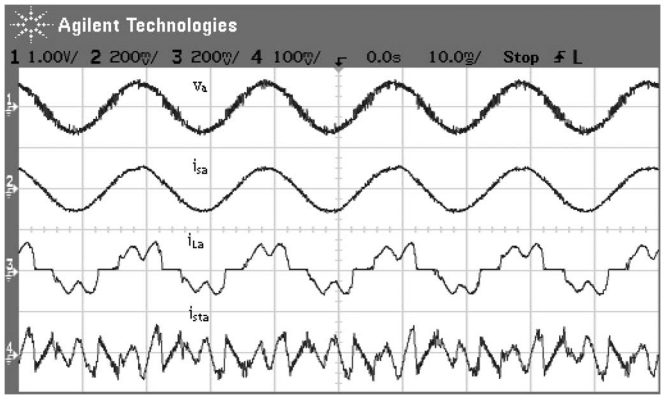


Fig. 10. Steady-state waveform showing phase-a quantities (scales: 150 V/div for channel 1, 20 A/div for channels 2 and 3, and 10 A/div for channel 4).

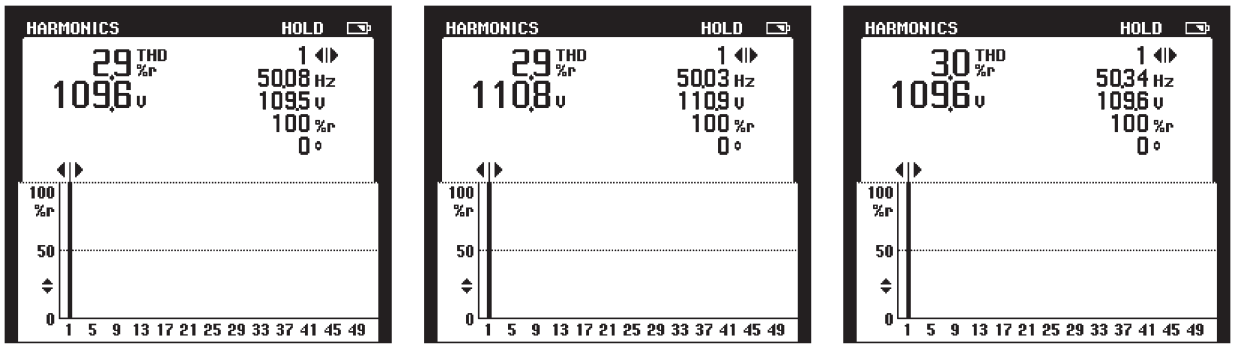
mitigation is being provided by the SAF during this condition. The load is increased to 1.2 kW at $t = 0.12$ s. At $t = 0.18$ s, the unbalance in the load is introduced. It can be seen from these waveforms of source currents that even if load currents are unbalanced and nonsinusoidal, the source currents are sinusoidal and balanced. The harmonic spectra of phase-a voltage, load current, and source current are shown in Fig. 5(a)–(c) for peak load condition. RMS and %THD values of voltage at PCC, load current, and source currents are given in Table II for light load, peak load, and unbalanced load conditions. Source currents and voltages are observed to be almost balanced and sinusoidal at unity power factor.

V. Hardware Results and Discussion

The performance of the SAF system with Adaline-based control is recorded with both linear and nonlinear loads. Furthermore, some results are presented to demonstrate the performance of control scheme. Load perturbations and transient performance of SAF are also discussed.

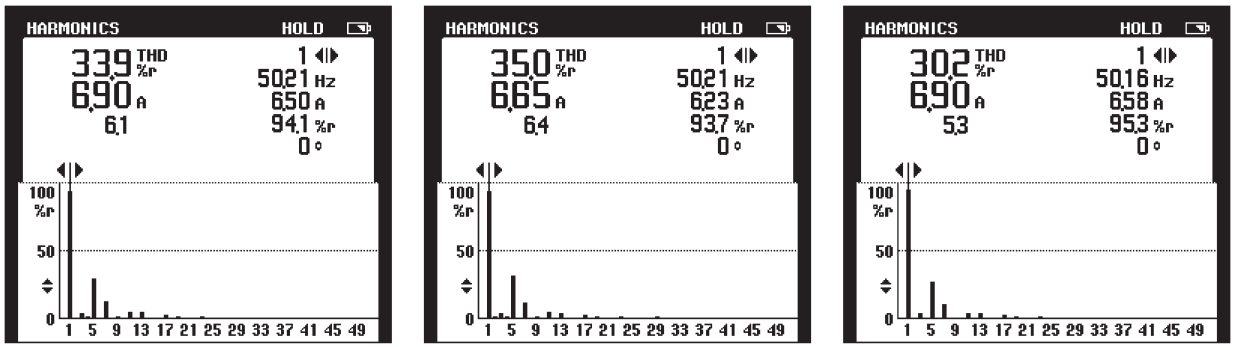
A. Performance of Adaline-Based Control Scheme

Estimation of reference current signals by Adaline requires generation of unit templates in phase with the phase voltage. The test is performed with a nonlinear load (diode bridge converter with capacitive filter at dc side) connected to the SAF system at 110-V line-to-line voltage. The nonlinear load distorts the voltage at PCC. Fig. 6 shows the phase-a voltage (v_a) with three-phase unit templates (u_a, u_b, and u_c). The distortion of phase-a voltage at PCC is clearly visible, whereas the unit templates are sinusoidal and undistorted. Furthermore, from the zero-crossing points, it can be seen that the phase-a unit voltage template is perfectly in phase with the



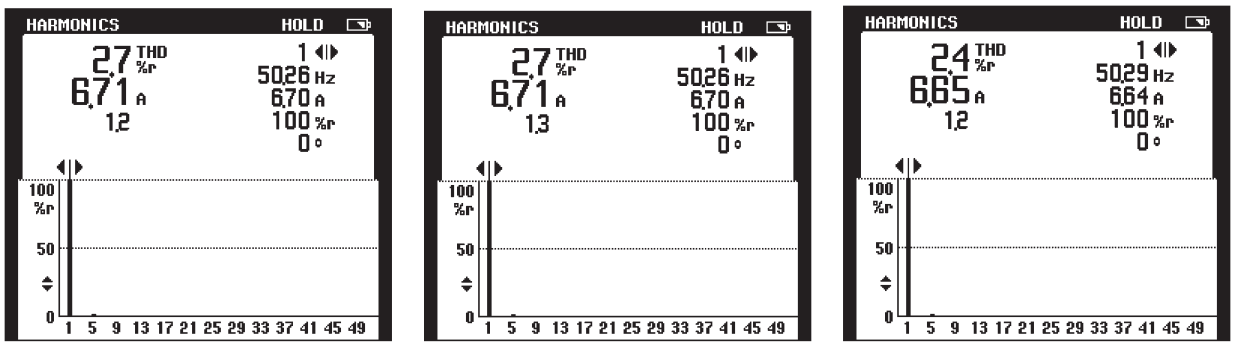
(a) (b) (c)

Fig. 11. Harmonic spectra of line-to-line (a) phase-a to phase-b voltage, (b) phase-b to phase-c voltage, and (c) phase-c to phase-a voltage.



(a) (b) (c)

Fig. 12. Harmonic spectra of (a) phase-a load current, (b) phase-b load current, and (c) phase-c load current.



(a) (b) (c)

Fig. 13. Harmonic spectra of (a) phase-a source current, (b) phase-b source current, and (c) phase-c source current.

phase-a voltage at PCC. Performance of the Adaline-based control scheme for decomposing the load currents and extracting real fundamental-frequency component of load currents is shown in Fig. 7. These signals recorded using a digital cathode ray oscilloscope (Agilent 54624A) show phase-a voltage (v_a), load current $(i_{\rm La})$, and extracted real fundamental-frequency part of current $(i_{\rm refa})$. Three-phase weights ($W_{\rm pa}$, $W_{\rm pb}$, and $W_{\rm pc}$) with equivalent average weight $(W_{\rm eq})$ are shown in Fig. 8.

From these experimental results, it can be observed that the generated unit templates are having unit amplitude and are well in phase with the respective three-phase voltages. The reference real fundamental-frequency current signals extracted using the Adaline-based technique are also well in phase with the voltages and contain only the real part of the load current. The equivalent weight and weights corresponding to the three phases shown in Fig. 8 are constant without any oscillations in averaged equivalent weight, and therefore, when multiplied by the undistorted unit voltage templates, it gives only the fundamental-frequency component in reference current.

B. Performance of SAF With Nonlinear Load

The experimental performance of the SAF with nonlinear load is presented to demonstrate its compensating characteristics. A diode bridge ac–dc converter with inductive–capacitive

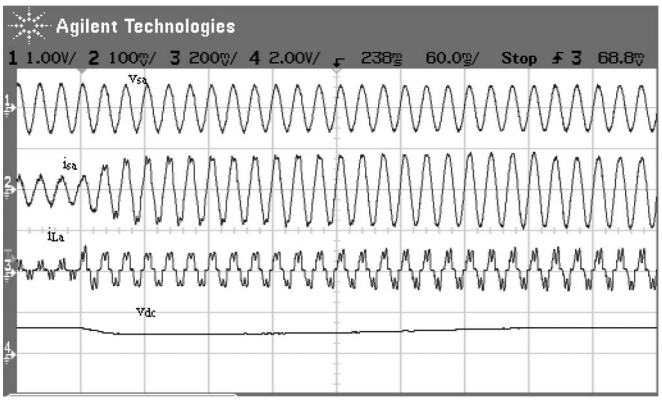


Fig. 14. Dynamic performance of SAF under load change (scales: 150 V/div for channel 1, 10 A/div for channel 2, 20 A/div for channel 3, and 300 V/div for channel 4).

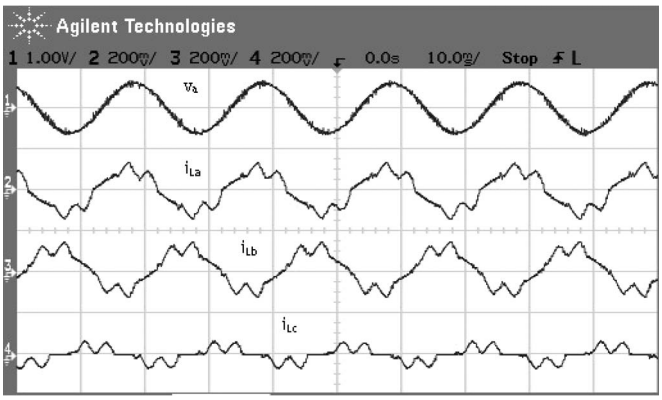


Fig. 15. Waveforms of three-phase currents of unbalanced and nonlinear loads (scales: 150 V/div for channel 1 and 20 A/div for channels 2, 3, and 4).

filter at dc side is chosen as the test load to study the operation of SAF for the load compensation. This load produces a constant voltage at dc side. The value of series inductance used is 1.4 mH. To have a 500-μF capacitance at dc side of the diode bridge converter, two ALCON-made 400-V 1000-μF capacitors are connected in series to provide higher voltage withstanding capability. The steady-state performance of the SAF providing reactive power and harmonic compensation is shown in Fig. 9. The waveforms shown in this figure are phase-a voltage, source current, load current, and dc bus voltage. The compensation provided to the load is clearly visible from the figure. The CRO trace showing a phase-a compensating current with other phase-a quantities is shown in Fig. 10. The recorded harmonic spectra of three-phase line-to-line voltages at PCC are shown in Fig. 11(a)–(c). Harmonic spectra of three-phase load currents are shown in Fig. 12(a)–(c). The total harmonic distortion (THD) in the load current is as high as 35%. Recorded harmonic spectra of source currents for all three phases are shown in Fig. 13(a)–(c). The harmonic content in the source current is 2.7%. Moreover, the source currents are well balanced with current values of 6.71, 6.71, and 6.65 A. %THD of source currents is less than 5%; therefore, it can be concluded that the SAF meets the %THD requirements set by IEEE519 standard [2].

The performance of the SAF to meet step change in the load is shown in Fig. 14. It can be observed that the dc bus voltage

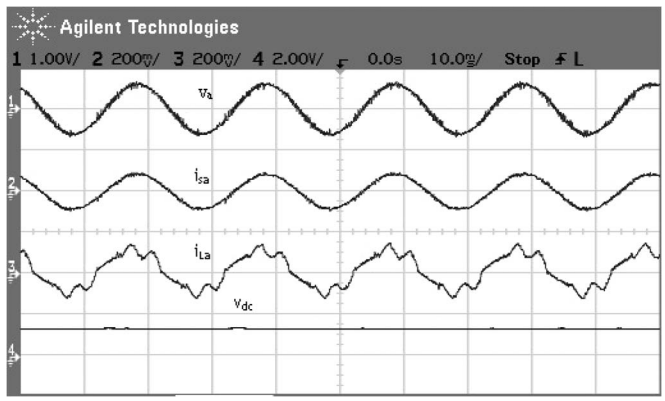


Fig. 16. Recorded steady-state waveform of compensation by SAF with unbalanced and nonlinear loads (scales: 150 V/div for channel 1, 20 A/div for channels 2 and 3, and 300 V/div for channel 4).

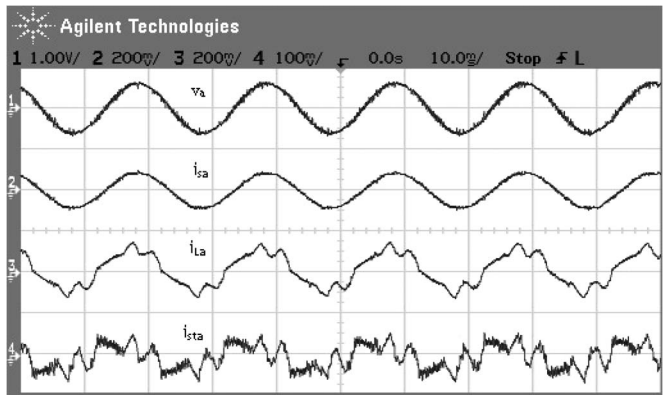


Fig. 17. Steady-state waveforms of phase-a quantities with unbalanced and nonlinear loads (scales: 150 V/div for channel 1, 20 A/div for channels 2 and 3, and 10 A/div for channel 4).

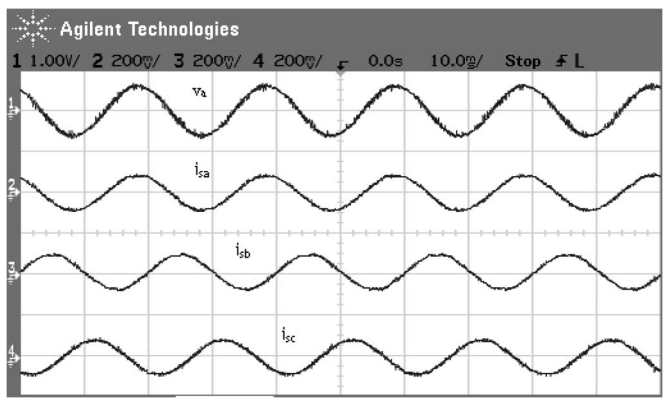
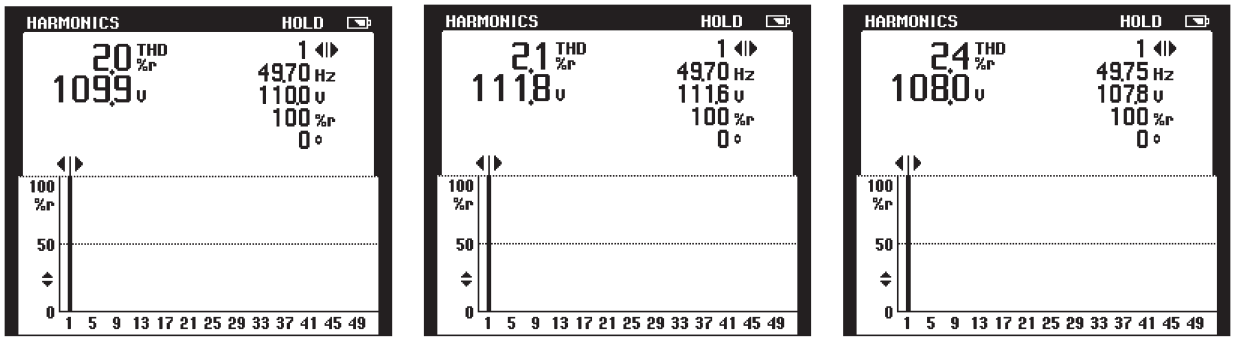


Fig. 18. Waveform of three-phase source currents with unbalanced and nonlinear loads (scales: 150 V/div for channel 1 and 20 A/div for channels 2, 3, and 4).

pf SAF settles to its steady-state value within a few cycles, and change in the load current is followed by the source current within one cycle of sine wave.

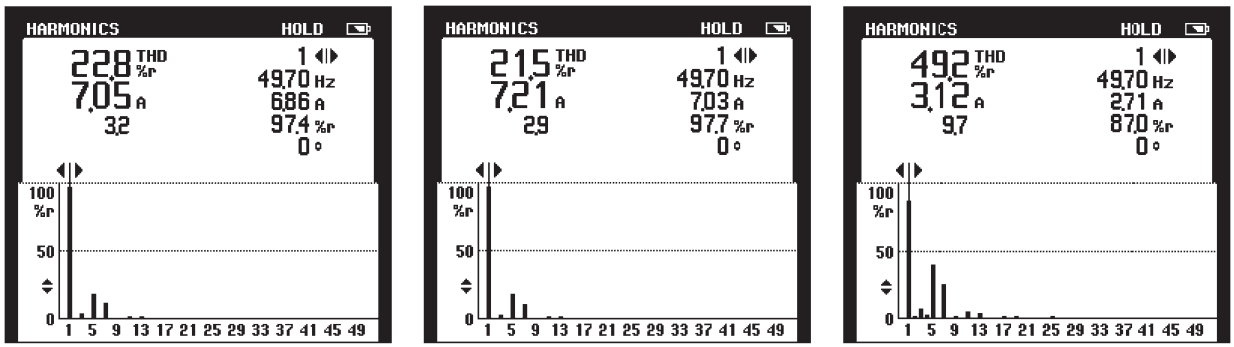
C. Performance of SAF With Unbalanced and Nonlinear Load

Fig. 15 shows the unbalanced and distorted three-phase load currents. The values of load currents of a, b, and c phases are 7.05, 7.21, and 3.12 A, respectively. A difference of more



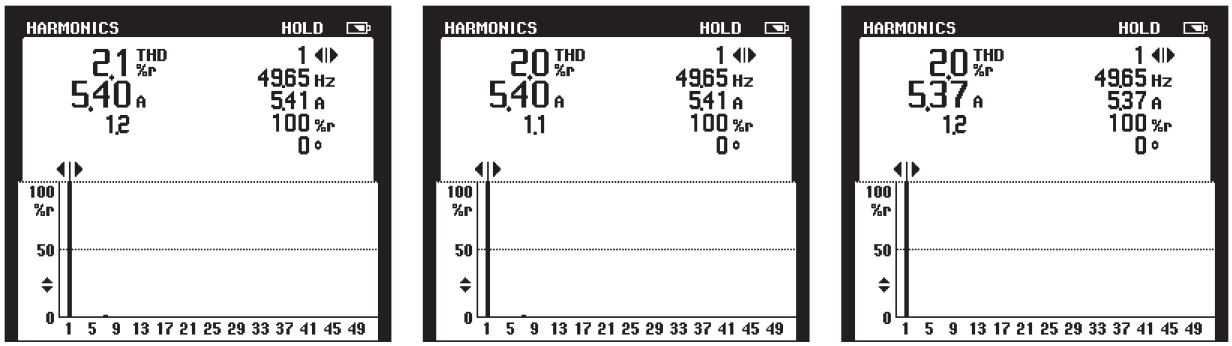
(a) (b) (c)

Fig. 19. Harmonic spectra of line-to-line (a) phase-a to phase-b voltage, (b) phase-b to phase-c voltage, and (c) phase-c to phase-a voltage.



(a) (b) (c)

Fig. 20. Harmonic spectra of (a) phase-a load current, (b) phase-b load current, and (c) phase-c load current.



(a) (b) (c)

Fig. 21. Harmonic spectra of (a) phase-a source current, (b) phase-b source current, and (c) phase-c source current.

than 4 A is between phase b and phase c, which gives an unbalance of more than 53%. The unbalance in the load is created by connecting a resistive load between phase a and phase b. The input line-to-line voltage is kept at 110 V, and the dc-link voltage of SAF is maintained at 200 V. Compensating characteristics of the SAF system are shown in Fig. 16. This figure shows the phase-a voltage, the source current, and the load current along with the dc-link voltage. Fig. 17 shows the voltage, the source current, and the load current along with SAF current corresponding to a phase. Fig. 18 shows the three-phase source currents along with the phase-a voltage. This figure shows that the source currents are balanced and sinusoidal even if the load is nonlinear and unbalanced.

The harmonic spectra with the data of rms values of the three-phase line-to-line voltages at PCC are shown in Fig. 19(a)–(c). The harmonic spectra of the three-phase load currents and source currents are shown in Figs. 20(a)–(c) and 21(a)–(c). The rms values of load currents are 7.05, 7.21, and 3.12 A (a difference of 4 A approximately) for a, b, and c phases, respectively. From the data provided in these traces, it can be concluded that source currents are well balanced with rms values of 5.40, 5.40, and 5.37 A. The THD in the load currents is brought down, in source currents by SAF, up to an extent of 2.0%. The THD value of these source currents is well below the limit of 5.0%, provided in standard IEEE519.

VI. Conclusion

An experimental verification of the suitability of the Adaline-based control algorithm for the SAF has been demonstrated

under various operating conditions. The operation of a SAF has been observed to be quite satisfactory with unbalanced and nonlinear loads. The simplicity of the control and the inherited linearity of the Adaline-based control are some of the salient features of the control algorithm. Moreover, it is clear from the presented results that a THD of as low as 2.5% is achieved for voltage source fed type of nonlinear loads. From these simulated and experimental results, it can be concluded that an SAF controlled by the Adaline technique is able to provide reactive power compensation, harmonic mitigation, and balancing of unbalanced and nonlinear loads.

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