Reactive Power Control in MMC HVDC System during ac Fault

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Abstract

This paper discusses the reactive power control in multiple modular converter (MMC) HVDC system during ac faults. A control methodology is proposed to solve the overcurrent during and after ac faults. Based on the proposed method, a control strategy is added to the MMC HVDC test to enable the Low Voltage Ride Through (LVRT) function of the converter. The effectiveness of the proposed method in supressing the overcurrent caused by the ac system interruption is verified using electromagnetic (EMT) simulation. The simulation also shows with the proposed LVRT control method, the converter can inject the desired reactive current to the ac system within its ability during the symmetric and asymmetric ac faults.

1 Introduction

Modular multi-level converter (MMC) based High Voltage Direct Current (HVDC) technology has become more and more competitive, especially for renewable energy integration. Each arm in an MMC consists of multiple modules (from dozens of levels up to hundreds of levels). These modules generate a multi-step sinusoidal waveform which has a very small harmonic distortion and a low switching frequency per device. These properties result in a lower power loss and filter rating compared to 2-level or 3-level Voltage Source Converters (VSC).

Like other VSCs, the active and reactive power of the MMC converter can also be controlled independently. Hence, the MMC converter can help regulate the ac system voltage by varying the output reactive power as long as it is within its capability curve.

How to control the reactive power of the MMC converter during the ac fault is an issue raised by the utility companies. Currently, the dq decoupling control method is applied in VSC control [1]. Without any control method, the MMC converter has an overcurrent issue during the ac fault and overvoltage in weak ac system after the fault is cleared. In addition, the grid operators require each converter connected to the grid to have a low-voltage-ride-through capability. This is another challenge for MMC reactive power control.

This paper presents a control method for an MMC converter to limit its reactive power output during 3-phase and single-phase ground fault. The HVDC scheme is considered to be of the symmetric monopole type. In this approach, only the positive sequence quantities are regulated during the 3-phase ground fault and negative sequence quantities regulated for the single-phase ground fault. The results, obtained by detailed EMT simulation, show that with this control strategy, the current on each arm is within acceptable limits during the symmetric and asymmetric ac fault and ac voltage is well regulated after the faults. This paper also presents a control strategy to realize an LVRT function on the MMC converter based on the EMT model.

2 Model Description

2.1 Main circuit

A generic symmetric monopole MMC HVDC scheme [2] is considered as shown in figure 1. It is used to test the control strategy. The HVDC converters are rated at ± 200kV, 500MW. The ac system at each terminal is represented by a Thevenin equivalent ac voltage source and ac impendence. The detailed parameters of the point-to-point MMC HVDC system are listed in table I.

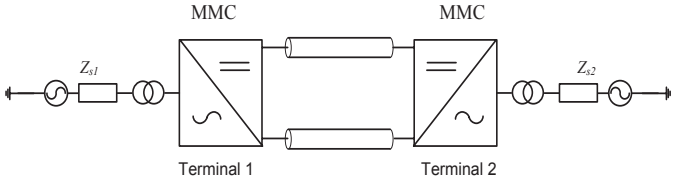

Figure 1: MMC HVDC test system

Table I
Parameters of MMC HVDC

Converter	Power	500MW
	Voltage	±200kV
	Level	201
	Cell capacitance	8000uF
Transformer	Rated Capacity	700MVA
	Leakage reactance	0.15
	Turns ratio	345kV/280kV
AC system	Frequency	60Hz
	X/R	10
	Short circuit current at terminal 1	3kA
	Short circuit current at terminal 2	4kA

Two underground dc cables [3] are used to transmit the power between terminal 1 and terminal 2. The detail parameters for the 200kV dc cable are given in figure 2.

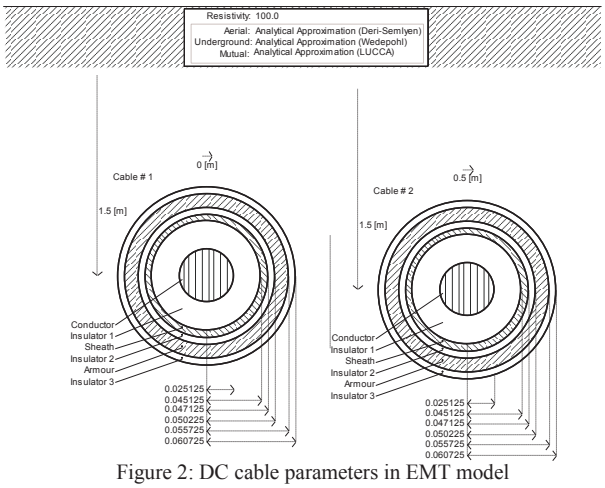

Figure 2: DC cable parameters in EMT model

2.2 Control system

The dq decoupling control shown in figure 3 is used in the test system to control the active and reactive power of each MMC converter. Terminal 1 is under constant active dc voltage/constant ac voltage control while terminal 2 is under constant active power/constant ac voltage control. All the inputs of control system are per-unitized.

The positive and negative sequence control strategy is adopted for the test system [1]. The positive sequence control is activated during the steady state or symmetric interruption in the ac system. The negative sequence control is only in effect when there is an asymmetric fault in the ac system. It monitors negative sequence currents from the MMC to the ac system and regulates them to the set point during the ac fault.

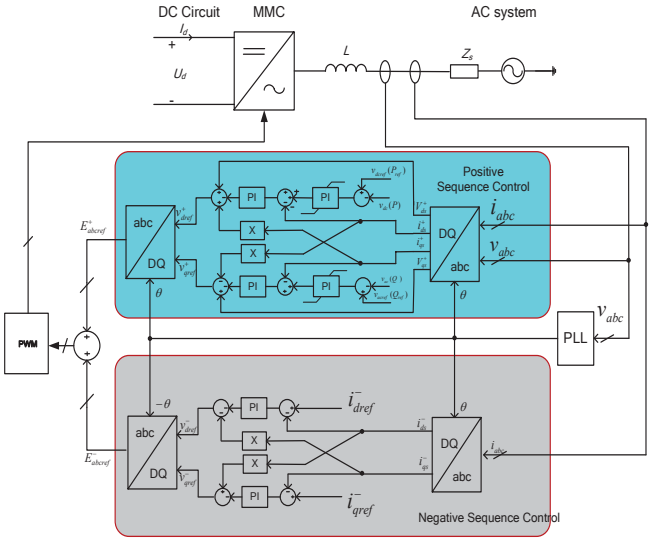

Figure 3: Control system for MMC converter

3 Reactive power control during ac fault

An ac fault is detected by monitoring the voltage on converter ac busbar. In this paper, the threshold value is set to 0.85pu. When the any phase voltage drops to the 0.85pu, the ac fault signals an 'ACUV' change from 0 to 1. Additional logic is required to distinguish between symmetric and asymmetric ac faults.

Without the control strategy discussed above, the PI controllers in the outer loop, i.e the power and ac voltage (or reactive) controllers which generate the id and iq orders for the inner loop, are too slow to regulate the fault current quickly, and hence cause overcurrent during the ac fault. Similarly, on fault clearance, they do not quickly restore the system voltage resulting in ac overvoltage in some weak ac system starts recovery. The figure 4 shows the overcurrent issue in the test after a 3LG fault on terminal 2 at 2.5s.

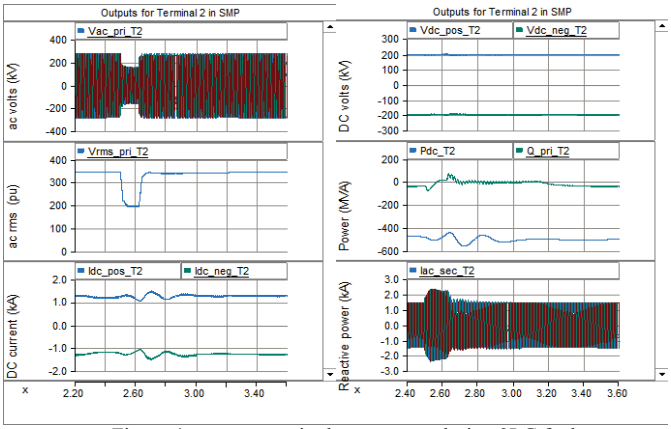

Figure 4: overcurrent in the converter during 3LG fault

In order to improve the performance of the MMC, the additional fast control strategy is used in the test system to limit the Id and Iq output of the converter after detecting the ac fault. As shown in figure 3, the PI controllers in the outer loop in the positive sequence control have an output limit function. In the steady state, the output limit is ± 1.5 pu. During the fault, the outputs of the PI controllers immediately reduce to zero by changing the output limit to zero. Consequently, the active and reactive power drops to zero. After the ac fault is cleared, and with certain delay, the output limit increases to its pre-fault value of 1.5. The change of the PI controller limit is as shown in figure 5.

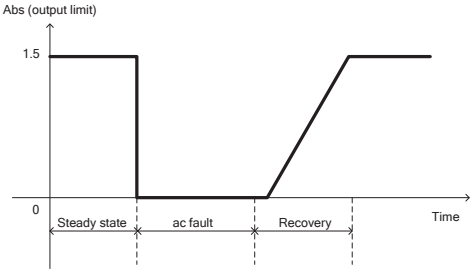

Figure 5: The change of the PI controller limit

In order to test this control strategy, a 120ms duration three-phase-to-ground fault is applied to the terminal 2 converter ac bus at t = 2.5s. The ac quantities at terminal 2 for this case are shown in figure 6. When a 120ms duration single-line-to-

ground fault is also applied at same location at 2.5s. The resultant traces for terminal 2 are plotted in figure 7. During the 3-phase-to-ground fault, the ac voltage drops to 200kV while the lowest line-to-line voltage is 288kV for the single-line-to-ground fault.

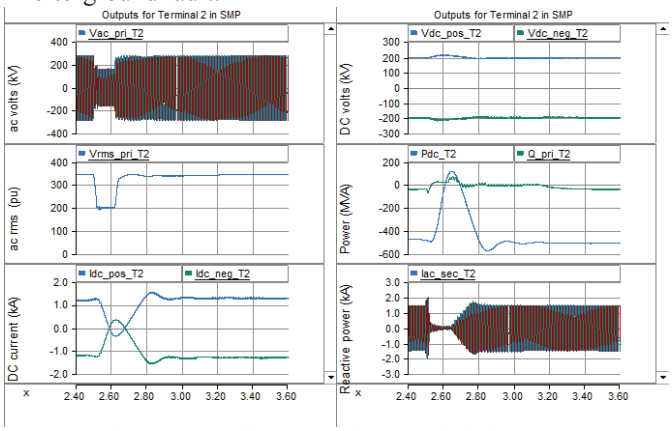

Figure 6: AC and DC quantities at terminal 2 in 3LG case

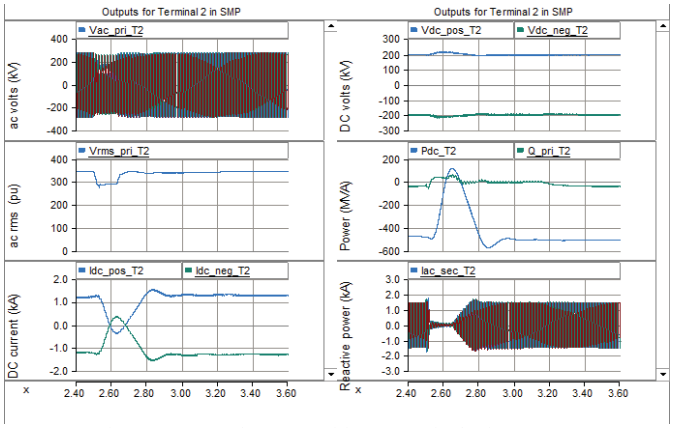

Figure 7: AC and DC quantities at terminal 2 in LG case

The results in figure 6 and 7 show that with the proposed control strategy, the converter in the MMC HVDC system has good performance during the ac fault and recovery period. By limiting the output of converters, the system does not have an overcurrent issue.

4 Reactive power control with LVRT ability

By limiting the active and reactive power to zero during the ac fault, the MMC converter has very good performance as seen from the simulation results. However, the grid operators desire the MMC converter to support ac voltage during the ac by generating reactive power (within its limit) instead of zero reactive power output.

The Low Voltage Ride though (LVRT) capability is related to the dynamic reactive power supporting of MMC converter during the ac fault. According to the European Electricity Network code, each HVDC system should have LVRT ability. The converter should remain connected to the network during the ac fault and continue stable operation after the system recover from the fault. Figure 8 shows the typical LVTR curve proposed in the European Electric Network code [4].

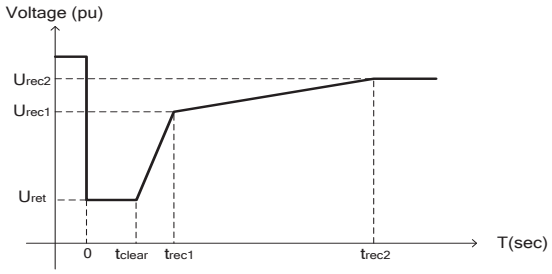

Figure 8: Typical LVRT curve

The diagram in Figure 8 shows the threshold voltage-against-time value during and after the ac fault to trip the HVDC converter. Uret is the sustained voltage during the fault. The (Urec1,trec1) and (Urec2,trec2) are specified coordinates of the lower limit of voltage recovery during recovery. Another requirement of the grid code is the reactive power compensation during the ac voltage sag. According to the grid code, the HVDC converter is required to provide reactive current compensation when the voltage deviation exceeds the threshold value ΔU, with the active current injection level relationship with the voltage deviation is shown in figure 9.

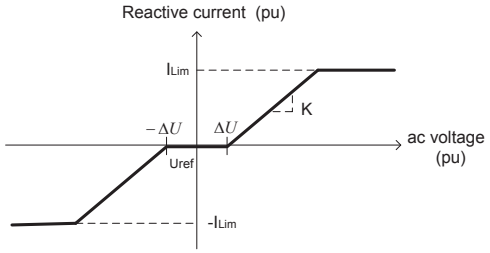

Figure 9: Reactive current compensation vs voltage deviation

4.1 Reactive power limitation of MMC converter

There are three main influence factors of the power capacity of VSC HVDC systems [5]: the maximum current limit of the IGBT, the maximum DC voltage level limit and the maximum DC current of the DC cable. The typical PQ curve of the VSC converter is shown in Figure 10. The diameter of the circle varies corresponding to different DC voltage.

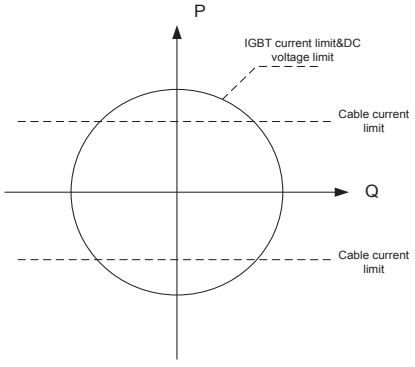

Figure 10 Typical PQ curve of VSC HVDC system

In this paper, the reactive current injection limit is sent to ±1.0pu to avoid the overcurrent in the converter. .

4.2 Reactive current compensation control during symmetric ac fault

During the symmetric ac fault, the outer loop PI controllers are set to zero by changing the PI limit value. Another modulation signal Δi^{+}_{qref} is added to the i_{qref} signal. The ac voltage rms value and 3-phase fault signal are used to generate Δi^{+}_{qref}. Hence, during the fault, only the inner loop PI controllers are used to maintain the zero active power output and provide the reactive current compensation.

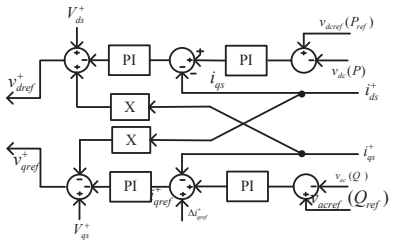

Figure 11 Positive sequence control with reactive current compensation

The control strategy in figure 11 is added in the test symmetric monopole MMC system. The slope k is set to 3 and the dead band ΔU=0.15pu in this case. A 3-phase-to-ground fault is applied at t =2.5s and last for 0.12s. The ac converter ac bus drops to 238kV rms during the ac fault.

Figure 12 shows all the quantities at terminal 2 from 2.4s to 3.6s. Before the ac fault, the system operates at its rated level. The active power is -500MW (converter at terminal 2 is acting as an inverter, feeding power to the ac network) while the reactive power is -50MVar. When the ac fault happens, the active power drops to zero and the converter starts to inject the active power to the ac system. Figure 13 plots the positive sequence and negative sequence Id and Iq orders from 2.4s to 3.6s. After detecting the 3-phase fault, only the positive sequence control reacts to the fault. The order Idref immediately reduces to zero while the Iqref jumps to -1.0pu to provide reactive current compensation to the ac system. After the fault is cleared, the converter returns rapidly back to its pre-fault level.

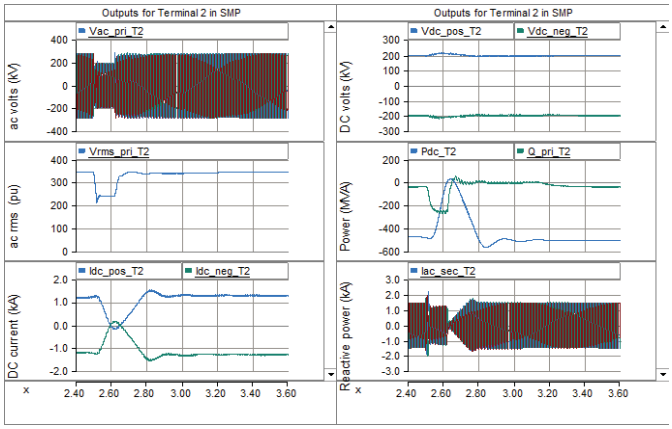

Figure 12: AC quantities at terminal 2 for 3LG fault

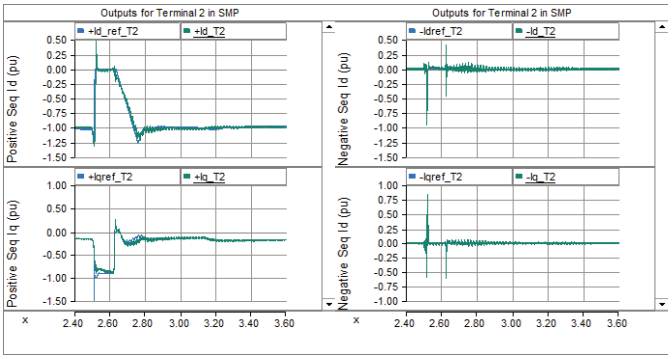

Figure 13: Id and Iq currents for 3LG fault

During the fault, due to reactive current injection, the converter outputs 250MVar reactive power to the system in this case. With this amount of reactive power support, the converter ac voltage increases from 200kV to 238kV during the fault.

4.3 Reactive current compensation control during asymmetric ac fault

During the asymmetric ac fault, Id and Iq orders in the positive sequence are set to zero. As shown in figure 14, another modulation signal Δi^{-}_{qref} is added to the $\Delta i'^{-}_{qref}$ signal. The phase rms voltage and fault signal are used to calculate Δi^{-}_{qref}.

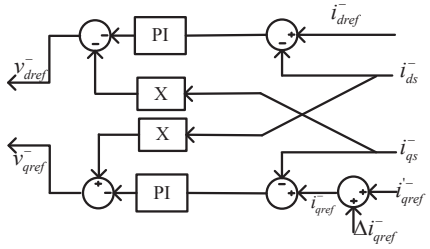

Figure 14 Negative sequence control with reactive current compensation

A single-line-to-ground fault is applied at terminal 2 converter ac bus at t=2.5s to test the LVRT function in the test system. The fault lasts for 120ms. The main quantities, including the instantaneous ac voltage, the rms voltage, the dc current and voltage, the active power and reactive power, the negative sequence Iq of the converter and the Iq order are recorded from 2.4s to 3.6s. Figure 15 shows the ac and dc quantities at terminal 2 and figure 16 plots the Id and Iq of the positive and negative sequence from 2.4s to 3.6s.

The traces in figure 15 show that during the single-line-to-ground fault that the converter at terminal 2 reduces the active power to zero, the line-to-line ac rms voltage drops to 298kV. The dc voltage remains constant. The converter starts to inject reactive power into the ac system on detecting the ac fault. After the fault, the ac voltage recovers to 345kV and the reactive power output returns -50MVar as its previous value.

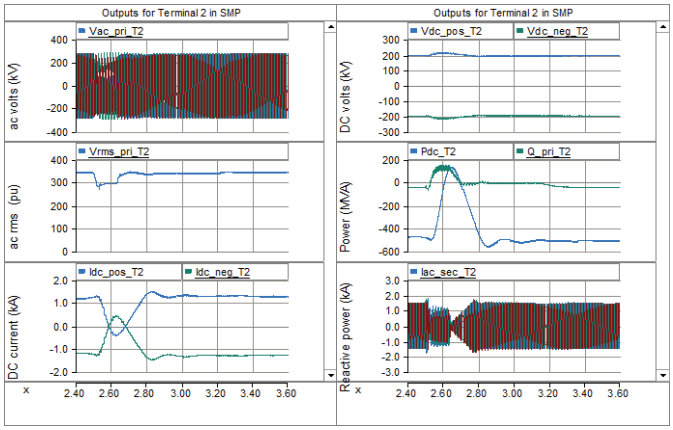

Figure 15: AC quantities at terminal 2 for LG fault

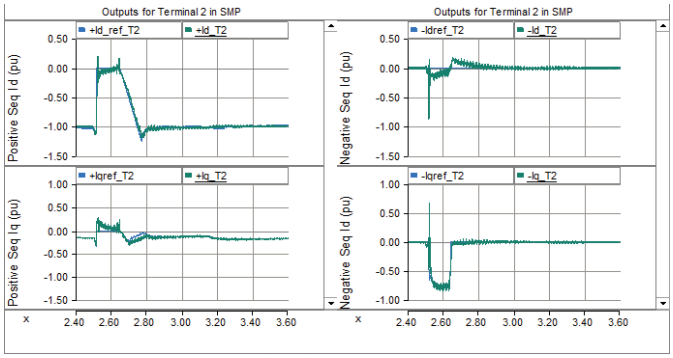

Figure 16: Id and Iq currents for LG fault

Figure 16 shows the MMC converter injects negative sequence reactive current to the ac sysem during the asymmetric ac fault. The Δi_{qref}^{-} reaches the limit and keeps constant. After the fault is cleared, the Δi_{qref}^{-} immediately drops to zero to avoid overvoltage at the ac bus. The LVRT function works as designed.

5 Conclusion

With a conventional VSC controller, the outer loop controllers is too slow and result in overcurrent during the fault. By dynamically limiting the outer loop PI controllers output, the MMC converter has better performance on reducing the overcurrent and voltage fluctuation. The positive and negative sequence dq decoupling control can smooth recovery from different types of ac fault. Finally, the LVRT scheme proposed in this paper can provide reactive current compensation as per grid code requirements during the symmetric and asymmetric ac faults. In a weak ac system (low SCR), the effect of reactive current compensation for support the ac voltage is significant.

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