Design of External Inductor for Improving Performance of Voltage Controlled DSTATCOM

Chandan Kumar, *Member, IEEE*, Mahesh K. Mishra, *Senior Member, IEEE* and Marco Liserre, *Fellow, IEEE*

***Abstract*—A distribution static compensator (DSTATCOM) is used for load voltage regulation and its performance mainly depends upon the feeder impedance and its nature (resistive, inductive, stiff, non-stiff). However, a study for analyzing voltage regulation performance of DSTATCOM depending upon network parameters is not well defined. This paper aims to provide a comprehensive study of design, operation, and flexible control of a DSTATCOM operating in voltage control mode. A detailed analysis of the voltage regulation capability of DSTATCOM under various feeder impedances is presented. Then, a benchmark design procedure to compute the value of external inductor is presented. A dynamic reference load voltage generation scheme is also developed which allows DSTATCOM to compensate load reactive power during normal operation, in addition to providing voltage support during disturbances. Simulation and experimental results validate the effectiveness of the proposed scheme.**

***Index Terms*—Distribution static compensator (DSTATCOM), current control, voltage control, power factor, power quality.**

I. Introduction

FAULTS in widespread power system as well as switching of large loads create voltage disturbances such as sag and swell in a distribution system [1]. These power quality (PQ) problems significantly degrade the performance of sensitive loads like process-control industry, electronics equipments, adjustable drives, etc.

Conventionally, static var compensator (SVC) is used to regulate load voltage, compensate reactive current, and improve transient stability. However, the SVC causes problems like harmonic current injection in the system, harmonic amplification, and possible resonance with the source impedance [2]. Distribution static compensator (DSTATCOM) has been proposed to overcome the limitations of SVC [3]–[9]. A DSTATCOM is one of the most effective solutions to regulate the load voltage. It provides load voltage regulation by supplying fundamental reactive current into source [5], [10]–[15].

However, most of the conventional DSTATCOMs used for voltage regulation consider highly inductive and/or significantly large feeder impedance [11], [13]. This is usually not true in a distribution system where feeder impedance used to be resistive in nature [16], [17]. In this scenario, the DSTATCOM will have small voltage regulation capability. Another important issue is the generation of reference load voltage. In conventional DSTATCOM application for voltage regulation, reference load voltage is set at 1.0 p.u. [13]. At this load voltage, VSI always exchanges reactive power with the source with leading power factor. This causes continuous power losses in the feeder and VSI. Also, a conventional DSTATCOM requires high current rating voltage source inverter (VSI) to provide voltage support [11]. This high current requirement increases the power rating of the VSI and produces more losses in the switches as well as in the feeder.

The voltage regulation performance of DSTATCOM mainly depends upon the feeder impedance and its nature (resistive, inductive, stiff, non-stiff). For voltage control mode (VCM) operation of DSTATCOM and/or grid connected inverters, the idea of inserting an external inductor in line has been reported [18], [19]. However, in these schemes, only the concept has been introduced leaving ample scope for further investigation and insight into the design details.

The focus of this paper is to provide a detailed design procedure for selecting the external inductor which satisfy several practical constraints, allows DSTATCOM to regulate load voltage in stiff as well as resistive feeder, reduce the current requirement for mitigation of sag, and reduce the system losses. With coordinated control of the load fundamental current, terminal voltage, and voltage across the external inductor, a dynamic reference load voltage generation scheme is presented. This scheme ensures unity power factor (UPF) operation during normal operation and maintains load voltage constant during voltage disturbances. Detailed simulation and experimental results are included to verify the DSTATCOM performance.

II. DSTATCOM in Power Distribution System

Fig. 1 shows power circuit diagram of the DSTATCOM topology connected in distribution system. L_s and R_s are source inductance and resistance, respectively. An external inductance, L_{ext} is included in series between load and source points. This inductor helps DSTATCOM to achieve load voltage regulation capability even in worst grid conditions, i.e., resistive or stiff grid. From IEEE-519 standard, point of common coupling (PCC) should be the point which is accessible to both the utility and the customer for direct measurement [20]. Therefore, the PCC is the point where L_{ext} is connected to the source. The DSTATCOM is connected at the point where load and L_{ext} are connected. The DSTATCOM uses a three-phase four-wire VSI. A passive LC filter is connected in each phase to filter out high frequency switching components. Voltages across dc capacitors, V_{dc1} and V_{dc2}, are maintained at a reference value of V_{dcref}.

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Chandan Kumar is with Electronics and Electrical Engineering Department, Indian Institute of Technology Guwahati, India (e-mail: chandank@iitg.ernet.in).

Mahesh K. Mishra is with Electrical Engineering Department, Indian Institute of Technology Madras, Chennai, India (e-mail: mahesh@ee.iitm.ac.in).

Marco Liserre is with Chair of Power Electronics, Christian-Albrechts-Universitat zu Kiel, Germany (e-mail: ml@tf.uni-kiel.de).

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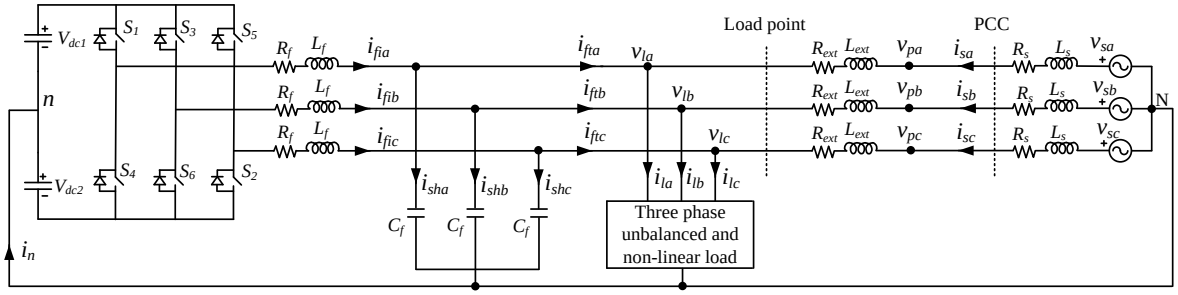

Fig. 1. Three phase equivalent circuit of DSTATCOM topology in distribution system.

III. Effect of Feeder Impedance on Voltage Regulation

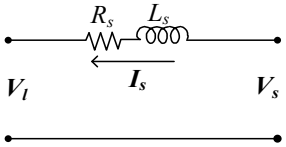

Fig. 2. Equivalent source-load model without considering external inductor.

To demonstrate the effect of feeder impedance on voltage regulation performance, an equivalent source-load model without considering external inductor is shown in Fig. 2. The current in the circuit is given as

$$\boldsymbol{I}_s = \frac{\boldsymbol{V}_s - \boldsymbol{V}_l}{\boldsymbol{Z}_s} \tag{1}$$

where $\boldsymbol{V}_s = V_s\angle\delta$, $\boldsymbol{V}_l = V_l\angle 0$, $\boldsymbol{I}_s = I_s\angle\phi$, and $\boldsymbol{Z}_s = Z_s\angle\theta_s$, with V_s, V_l, I_s, Z_s, δ, ϕ, and θ_s are rms source voltage, rms load voltage, rms source current, feeder impedance, load angle, power factor angle, and feeder impedance angle, respectively. The three phase average load power (P_l) is expressed as

$$P_l = Real\left[3\,\boldsymbol{V}_l \times \boldsymbol{I}_s{}^*\right]. \tag{2}$$

Substituting $\boldsymbol{V}_l$ and $\boldsymbol{I}_s$ in (2), the load active power is

$$P_l = \frac{3\,V_l^2}{Z_s}\left[\frac{V_s}{V_l}\cos(\theta_s - \delta) - \cos\,\theta_s\right]. \tag{3}$$

Rearranging (3), expression for δ is computed as follows:

$$\delta = \theta_s - \cos^{-1}\left[\frac{V_l}{V_s}\left(\cos\,\theta_s + \frac{P_l Z_s}{3\,V_l^2}\right)\right]. \tag{4}$$

For power transfer from source to load with stable operation in an inductive feeder, δ must be positive and less than $90°$. Also, all the terms of the second part of (4), i.e., inside $\cos^{-1}$, are amplitude and will always be positive. Therefore, value of the second part will be between '0' to '$\pi/2$' for the entire operation of the load. Consequently, the load angle will lie between θ_s to (θ_s - $\pi/2$) under any load operation, and therefore, maximum possible load angle is θ_s.

The vector expression for source voltage is given as follows:

$$\boldsymbol{V_s} = V_l + I_s Z_s\angle\left(\theta_s + \phi\right). \tag{5}$$

A DSTATCOM regulates the load voltage by injecting fundamental reactive current. To demonstrate the DSTATCOM voltage regulation capability at different supply voltages for different R_s/X_s, vector diagrams using (5) are drawn in Fig. 3. To draw diagrams, load voltage V_l is taken as reference phasor having the nominal value OA (1.0 p.u.). With aim of making V_l = V_s = 1.0 p.u., locus of V_s will be a semicircle of radius V_l. Since, the maximum possible load angle is $90°$ in an inductive feeder, phasor $\boldsymbol{V_s}$ can be anywhere inside curve $OACBO$. It can be seen that the value of $\theta_s + \phi$ must be greater than $90°$ for zero voltage regulation. Additionally, it is possible only when power factor is leading at the load terminal as θ_s cannot be more than $90°$.

Fig. 3(a) shows the limiting case when R_s/X_s = 1, i.e., θ_s = $45°$. From (4), the maximum possible load angle is $45°$. The maximum value of angle, $\theta_s + \phi$, can be $135°$ when ϕ is $90°$. Hence, the limiting source current phasor OE, which is denoted by I_{slimit}, will lead the load voltage by $90°$. Lines OC and AB show the limiting vectors of V_s and $I_s Z_s$, respectively with D as the intersection point. Hence, area under $ACDA$ shows the operating region of DSTATCOM for voltage regulation. The point D has a limiting value of V_{slimit} = $I_s Z_s$ = 0.706 p.u. Therefore, maximum possible voltage regulation is 29.4%. However, it is impossible to achieve these two limits simultaneously as δ and ϕ cannot be maximum at the same time. Again if Z_s is low then source current, which will be almost inductive, will be enough to be realized by a DSTATCOM.

Fig. 3(b) considers case when R_s/X_s = $\sqrt{3}$ i.e., θ_s = $30°$. The area under $ACDA$ shrinks, which shows that with the increase in R_s/X_s from the limiting value, the voltage regulation capability decreases. In this case the limiting values of V_{slimit} and $I_s Z_s$ are found to be 0.866 and 0.5 p.u., respectively. Here, maximum possible voltage regulation is 13.4%. However, due to high current requirement, a practical DSTATCOM can provide very small voltage regulation.

Voltage regulation performance curves for more resistive grid, i.e., θ_s = $15°$, as shown in Fig. 3(c), can be drawn similarly. Here, area under $ACDA$ is negligible. For this case, hardly any voltage regulation is possible. Therefore, more the feeder is resistive in nature, lesser will be the voltage regulation capability.

Therefore, it is inferred that the voltage regulation capability of DSTATCOM in a distribution system mainly depends upon the feeder impedance. Due to resistive nature of feeder in a

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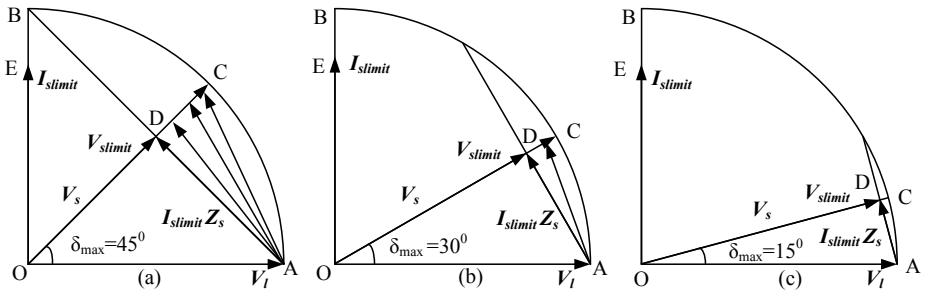

Fig. 3. Voltage regulation performance curve of DSTATCOM at different R_s/X_s. (a) For R_s/X_s = 1. (b) For R_s/X_s = $\sqrt{3}$. (c) For R_s/X_s = 3.73.

distribution system, DSTATCOM voltage regulation capability is limited. Moreover, very high current is required to mitigate small voltage disturbances which results in higher rating of IGBT switches as well as increased losses. One more point worth to be noted is that, in the resistive feeder, there will be some voltage drop in the line at nominal source voltage which the DSTATCOM may not be able compensate to maintain load voltage at 1.0 p.u. even with an ideal VSI.

IV. Selection of External Inductor for Voltage Regulation Improvement and Rating Reduction

This section presents a generalized procedure to select external inductor for improvement in DSTATCOM voltage regulation capability while reducing the current rating of VSI. Fig. 4 shows single phase equivalent DSTATCOM circuit diagram in distribution system. With balanced voltages, source current will be

$$\boldsymbol{I}_s = \frac{V_s\angle\delta - V_l\angle 0}{(R_s + R_{ext}) + j\,(X_s + X_{ext})} = \frac{V_s\angle\delta - V_l\angle 0}{R_{sef} + jX_{sef}} \quad (6)$$

where $R_{sef} = R_s + R_{ext}$ and $X_{sef} = X_s + X_{ext}$ are effective feeder resistance and reactance, respectively. R_{ext} is equivalent series resistance (ESR) of external inductor, and will be small. With $\theta_{sef} = \tan^{-1}\frac{X_{sef}}{R_{sef}}$ and $Z_{sef} = \sqrt{R_{sef}^2 + X_{sef}^2}$ as effective impedance angle and effective feeder impedance, respectively, the imaginary component of $\boldsymbol{I}_s$ is given as

$$I_s^{im} = \frac{V_l \sin\theta_{sef} + V_s \sin(\delta - \theta_{sef})}{Z_{sef}}. \quad (7)$$

With the addition of external impedance, the effective feeder impedance becomes predominantly inductive. Hence, $Z_{sef} \approx X_{sef}$. Therefore, approximated I_s^{im} will be

$$I_s^{im} = \frac{V_l \sin\theta_{sef} + V_s \sin(\delta - \theta_{sef})}{X_{sef}}. \quad (8)$$

DSTATCOM Power rating (S_{vsi}) is given as follows [21]:

$$S_{vsi} = \sqrt{3}\,\frac{V_{dc}}{\sqrt{2}}\,I_{vsi} \quad (9)$$

where I_{vsi} is the rms phase current rating of the VSI and V_{dc} is the voltage maintained at the dc capacitors. The DSTATCOM aims to inject harmonic and reactive current component of load currents. Suppose I_l^{im} is the maximum rms reactive and harmonic current rating of the load, then the value of

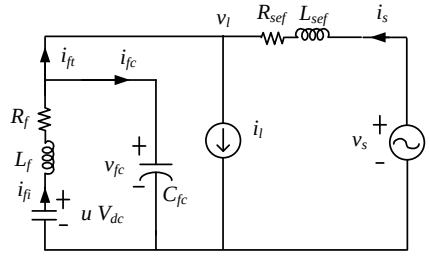

Fig. 4. Single phase equivalent circuit of DSTATCOM topology with external inductor in distribution system.

compensator current used for voltage regulation (same as I_s^{im}) is obtained by subtracting I_l^{im} from I_{vsi} and given as follows:

$$I = I_{vsi} - I_l^{im} = \frac{\sqrt{2}S_{vsi}}{\sqrt{3}V_{dc}} - I_l^{im}. \quad (10)$$

Comparing (8) and (10) while using value of δ from (4), following expression is obtained:

$$X_{sef} = \frac{V_l \sin\theta_{sef} - V_s \sin\left[\cos^{-1}\left[\frac{V_l}{V_s}\left(\cos\,\theta_{sef} + \frac{P_l X_{sef}}{3\,V_l^2}\right)\right]\right]}{\frac{\sqrt{2}S_{vsi}}{\sqrt{3}V_{dc}} - I_l^{im}}. \quad (11)$$

The above expression is used to compute the value of external inductor. Design example of external inductor, used for this work, is given in next section.

V. Design Example of External Inductor

Here, it is assumed that the considered DSTATCOM protects load from a voltage sag of 60%. Hence, source voltage V_s = 0.6 p.u. is considered as worst case voltage disturbances. During voltage disturbances, the loads should remain operational while improving the DSTATCOM capability to mitigate the sag. Therefore, the load voltage during voltage sag is maintained at 0.9 p.u., which is sufficient for satisfactory operation of the load. In the present case, maximum required value of I_l^{im} is 10 A. With the system parameters given in Table I, the effective reactance after solving (11) is found to be 2.2 Ω (L_{sef} = 7 mH). Hence, value of external inductance, L_{ext}, will be 6.7 mH. This external inductor is selected while satisfying the constraints such as maximum load power demand, rating of DSTATCOM, and amount of sag to be mitigated. In this design example, for base voltage and base power rating of 400

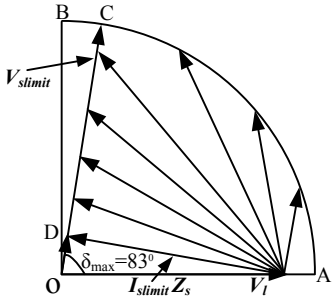

Fig. 5. Voltage regulation performance of DSTATCOM with external inductance.

TABLE I
SIMULATION PARAMETERS

System quantities	Values
Source voltage	230 V rms L-N (1.0 p.u.), 50 Hz
Feeder impedance	R_s = 0.3 Ω, L_s = 0.3 mH, R_s/X_s = 3.185
External impedance	L_{ext} = 6.7 mH, R_{ext} = 0.07 Ω
Linear load	Z_{la} = 30 + j62.8 Ω, Z_{lb} = 40 + j78.5 Ω, Z_{lc} = 50 + j50.24 Ω
Nonlinear load	Three phase rectifier supplying R-L load of 50 Ω and 200 mH
VSI parameters	V_{dc} = 520 V, C_{dc} = 2600 μF, L_f = 5 mH, C_f = 20 μF, S_{vsi} = 30 kVA
PI gains	$K_{p\delta}$ = 8.5 e^{-7}, $K_{i\delta}$ = 1.8 e^{-6}

V and 10 kVA, respectively, the value of external inductance is 0.13 p.u. Moreover, with total inductance of 7 mH (external and actual grid inductance), the total impedance will be 0.137 p. u. The short circuit capacity of the line will be 1/0.13 = 7.7 p.u. which is sufficient for the satisfactory operation of the system. Additionally, a designer always has flexibility to find suitable value of L_{ext} if the constraints are modified or circuit conditions are changed. Moreover, conventional DSTATCOM operated for achieving voltage regulation uses large feeder inductances [11], [13].

With the external inductance while neglecting its ESR, R_s/X_{sef} will be 0.13 i.e., θ_{sef} = 83°. Voltage regulation performance curves of the DSTATCOM in this case are shown in Fig. 5, where the area under $ACDA$ covers the majority of the stable operating range $OABO$. Hence, introduction of external inductor greatly improves the DSTATCOM voltage regulation capability. Additionally, due to increased effective feeder impedance the current requirement for sag mitigation also reduces. Moreover, if ESR of the external inductor is included, then the equivalent feeder impedance angle changes slightly (i.e., from 83 degree to 80.45 degree), and has negligible effect on the expression obtained in (11) as well as the voltage regulation capability of the DSTATCOM.

VI. FLEXIBLE CONTROL STRATEGY

This sections presents a flexible control strategy to improve the performance of DSTATCOM in presence of the external inductor L_{ext}. Firstly, a dynamic reference load voltage based on the coordinated control of the load fundamental current, PCC voltage, and voltage across the external inductor is computed. Then, a proportional integral (PI) controller is used to control the load angle which helps in regulating the dc bus voltage at a reference value. Finally, three phase reference load voltages are generated. The block diagram of the control strategy is shown in Fig. 6.

A. Derivation of Dynamic Reference Voltage Magnitude (V_l^*)

In conventional VCM operation of DSTATCOM, the reference load voltage is maintained at a constant value of 1.0 p.u. [10]–[12]. Source currents cannot be controlled in this reference generation scheme. Therefore, power factor will not be unity and source exchanges reactive power with the system even at nominal supply. To overcome this limitation, a flexible control strategy is developed to generate reference load voltage. This scheme allows DSTATCOM to set different reference voltages during various operating conditions. The scheme is described in the following.

1) Normal Operation: It is defined as the condition when load voltage lies between 0.9 to 1.1 p.u. In this case, the proposed flexible control strategy controls load voltages such that the source currents are balanced sinusoidal and VSI does not exchange any reactive power with the source. Hence, the source supplies only fundamental positive sequence current component to support the average load power and VSI losses. Reference source currents (i_{sj}^* where $j = a, b, c$ are three phases), computed using instantaneous symmetrical component theory [22], are given as

$$i_{sj}^* = \frac{v_{pj1}^+}{\Delta_1^+}(P_l + P_{loss}) \tag{12}$$

where $\Delta_1^+ = \sum_{j=a,b,c}(v_{pj1}^+)^2$. The voltages v_{pa1}^+, v_{pb1}^+, and v_{pc1}^+ are fundamental positive sequence components of PCC voltages. Average load power (P_l) and VSI losses (P_{loss}) are calculated using moving average filter (MAF) as follows:

$$P_l = \frac{1}{T}\int_{t_1-T}^{t_1}(v_{la}i_{la} + v_{lb}i_{lb} + v_{lc}i_{lc})\,dt \tag{13}$$

$$P_{loss} = \frac{1}{T}\int_{t_1-T}^{t_1}(v_{la}i_{fta} + v_{lb}i_{ftb} + v_{lc}i_{ftc})\,dt. \tag{14}$$

The reference source currents must be in phase with the respective phase fundamental positive sequence PCC voltages for achieving UPF at the PCC. Instantaneous PCC voltage and reference source current in phase-a can be defined as follows:

$$v_{pa1}^+ = \sqrt{2}\,V_{pa1}^+\sin(\omega t - \varphi_{pa1}^+),\ i_{sa}^* = \sqrt{2}\,I_{sa}^*\sin(\omega t - \varphi_{pa1}^+) \tag{15}$$

where V_{pa1}^+ and φ_{pa1}^+ are rms voltage and angle of fundamental positive sequence voltage in phase-a, respectively. I_{sa}^* is the rms reference source current obtained from (12). With external impedance, the expected load voltage is given as follows:

$$\boldsymbol{V}_{la} = \boldsymbol{V}_{pa1}^+ - \boldsymbol{I}_{sa}^*\,Z_{ext}. \tag{16}$$

From (15) and (16), the load voltage magnitude will be

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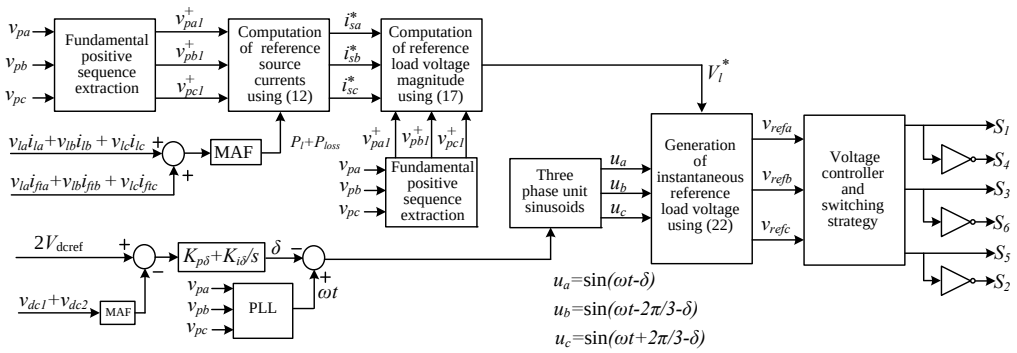

Fig. 6. Block diagram of proposed flexible control strategy.

$$V_{la} = \sqrt{\left[\left(V_{pa1}^{+}\cos\varphi_{pa1}^{+} - I_{sa}^{*}\,Z_{ext}\cos\left(\theta_{ext}-\varphi_{pa1}^{+}\right)\right)^{2} + \left(V_{pa1}^{+}\sin\varphi_{pa1}^{+} - I_{sa}^{*}\,Z_{ext}\sin\left(\theta_{ext}-\varphi_{pa1}^{+}\right)\right)^{2}\right]}. \quad (17)$$

With UPF at the PCC, the voltage across the external inductor will lead the PCC voltage by 90°. Neglecting ESR of external inductor, it can be observed that the voltage across external inductor improves the load voltage compared to the PCC voltage. This highlights another advantage of external inductor where it helps in improving the load voltage. As long as V_{la} lies between 0.9 to 1.1 p.u., same voltage is used as reference terminal voltage (V_l^*), i.e.,

$$\text{if } V_{la} \in [0.9 - 1.1 \text{ p.u.}], \text{ then } V_l^* = V_{la}. \quad (18)$$

2) Operation During Sag: Voltage sag is considered when value of (17) is less than 0.9 p.u. To keep filter current minimum, the reference voltage is set to 0.9 p.u. Therefore,

$$V_l^* = 0.9 \text{ p.u.} \quad (19)$$

3) Operation During Swell: A voltage swell is considered when any of the PCC phase voltage exceeds 1.1 p.u. In this case, reference load voltage (V_l^*) is set to 1.1 p.u. which results in minimum current injection. Therefore,

$$V_l^* = 1.1 \text{ p.u.} \quad (20)$$

B. Computation of Load Angle (δ)

Average real power at the PCC (P_{pcc}) is sum of average load power (P_l) and VSI losses (P_{loss}). The real power P_{pcc} is taken from the source depending upon the angle between source and load voltages, i.e., load angle δ. If DSTATCOM dc bus capacitor voltage is regulated to a reference value, then in steady state condition P_{loss} is a constant value and forms a fraction of P_{pcc}. Consequently, δ is also a constant value.

The dc link voltage is regulated by generating a suitable value of δ. The average voltage across dc capacitors (V_{dc1} + V_{dc2}) is compared with a reference voltage and error is passed through a PI controller. Output of PI controller, δ, is given as

$$\delta = K_{p\delta}\, e_{vdc} + K_{i\delta} \int e_{vdc}\, dt \quad (21)$$

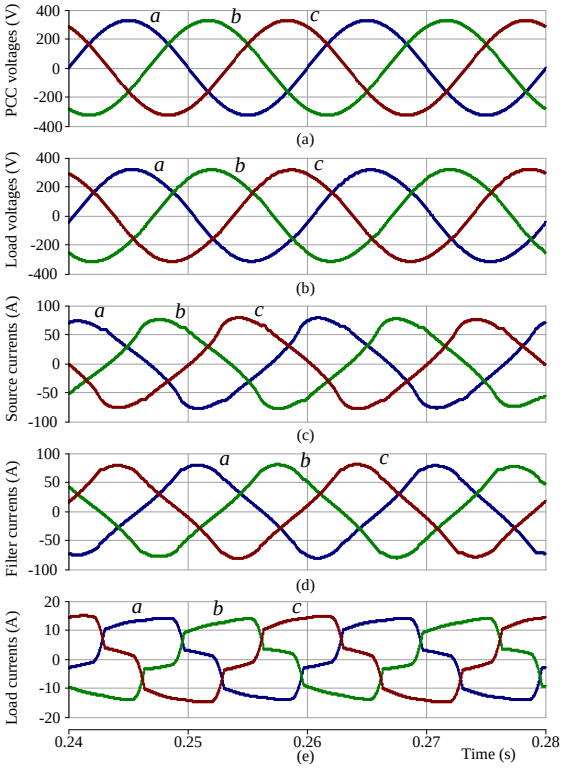

Fig. 7. Voltage regulation performance of conventional DSTATCOM with resistive feeder. (a) PCC voltages. (b) Load Voltages. (c) Source currents. (d) Filter currents. (e) Load currents.

where $e_{vdc} = 2\,V_{dcref} - (V_{dc1} + V_{dc2})$ is the voltage error. $K_{p\delta}$ and $K_{i\delta}$ are proportional and integral gains, respectively.

C. Generation of Instantaneous Reference Voltage

Selecting suitable reference load voltage magnitude and computing load angle δ from (21), the three phase balanced sinusoidal reference load voltages are given as follows:

$$\begin{aligned} v_{refa} &= \sqrt{2}\,V_l^*\,\sin(\omega t - \delta) \\ v_{refb} &= \sqrt{2}\,V_l^*\,\sin(\omega t - 2\pi/3 - \delta) \\ v_{refc} &= \sqrt{2}\,V_l^*\,\sin(\omega t + 2\pi/3 - \delta). \end{aligned} \quad (22)$$

These voltages are realized by the VSI using a predictive voltage controller [23].

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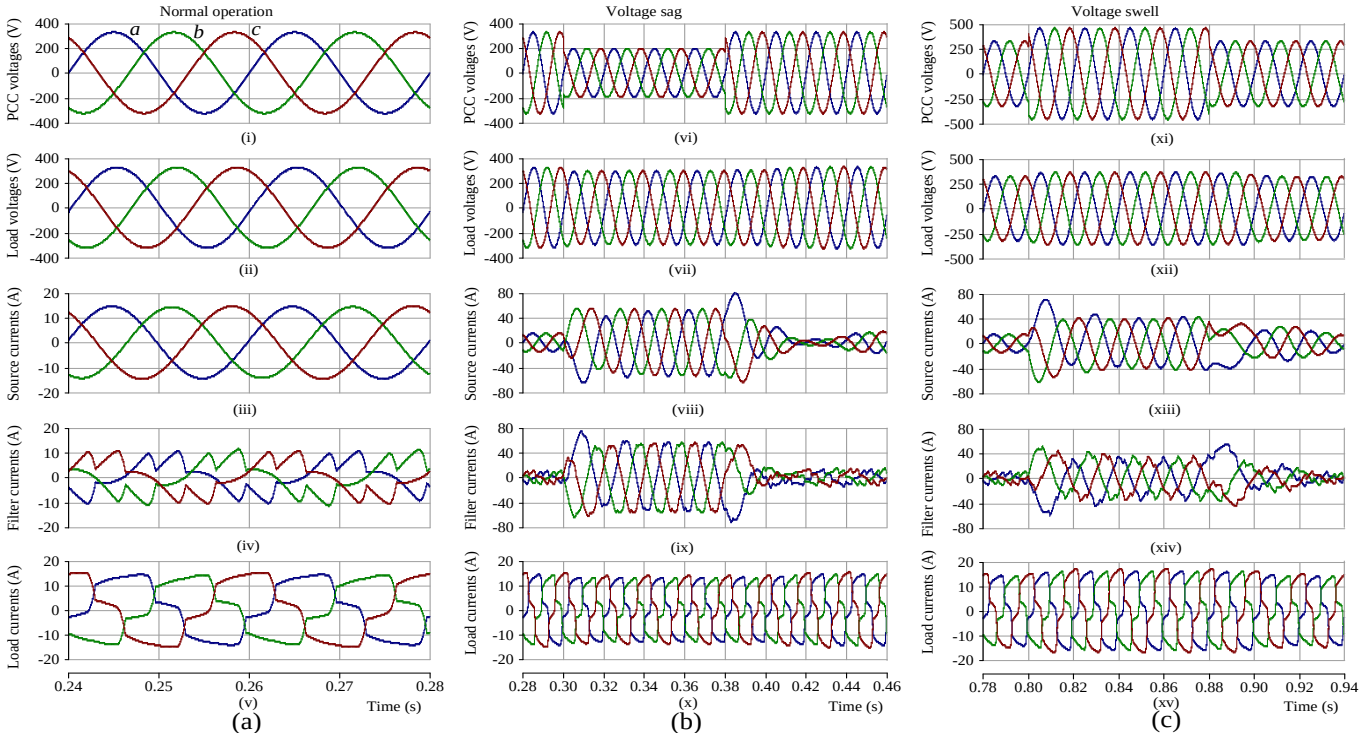

Fig. 8. Simulation results. (a) During normal operation (i)-(v). (b) During voltage sag (vi)-(x). (c) During voltage swell (xi)-(xv).

VII. Simulation Results

The parameters of DSTATCOM compensated distribution system are given in Table I. Usual scenario in distribution system having resistive feeder impedance is considered. PSCAD software is used to simulate the system. Firstly, the DSTATCOM is operated in conventional VCM, i.e., 1) without external inductor and 2) with a reference voltage of 1.0 p.u. or 230 V rms. The steady state waveforms of three phase PCC voltages, load voltages, source currents, filter currents, and load currents are shown in Figs. 7(a)-(e), respectively. Here, the DSTATCOM has to compensate only for feeder drop. However, from the load voltage waveform shown in Fig. 7(b), its magnitude is found to be 227.7 V. It confirms that the DSTATCOM has limited voltage regulation capability in a resistive feeder. It can be noticed from Fig. 7(c) that the magnitude of source current is very large and almost leading load voltage by 90°. This large reactive current is supplied by the VSI, as shown in Fig. 7(d), which increases its current rating. These waveforms confirm that a DSTATCOM cannot provide voltage regulation in resistive feeder, requires high current rating VSI for small voltage regulation, and exchanges reactive power with source even at nominal operation. Further, the high current produces excessive losses in the system.

Figs. 8(i)-(v) provide the steady state waveforms with the designed external inductance and flexible control strategy. This scheme simultaneously controls load voltages and source currents. The three phase normal PCC voltages are shown in Fig. 8(i). The load voltages and source currents waveforms are shown in Figs. 8(ii) and (iii), respectively. These waveforms are balanced and sinusoidal. Also, UPF is achieved at the PCC. Hence, compensator supplies only load harmonic and reactive

TABLE II
Experimental Setup Parameters

System quantities	Values
Source voltage	50 V rms L-N (1.0 p.u.), 50 Hz
Feeder impedance	R_s = 0.3 Ω, L_s = 0.3 mH, R_s/X_s = 3.185
External impedance	L_{ext} = 6.7 mH, R_{ext} = 0.07 Ω
Linear load	Z_{la} = 30 + j31.4 Ω, Z_{lb} = 40 + j16 Ω, Z_{lc} = 50 + j31.4 Ω
Nonlinear load	Three phase rectifier supplying R-L load of 50 Ω and 100 mH
VSI parameters	V_{dc} = 130 V, C_{dc} = 2600 μF, L_f = 5 mH, C_f = 20 μF

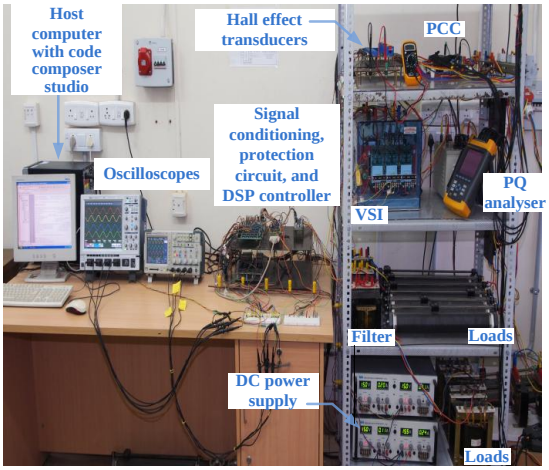

Fig. 9. Photograph of experimental setup.

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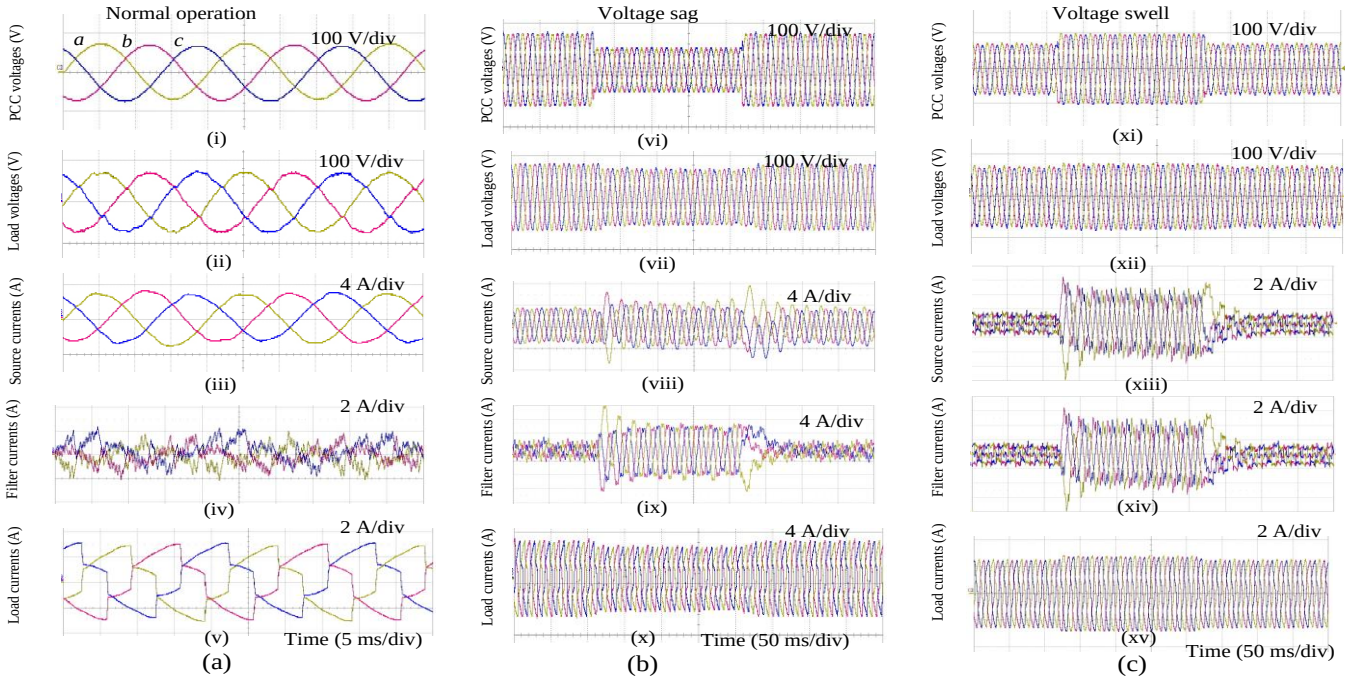

Fig. 10. Experimental results. (a) During normal operation (i)-(v). (b) During voltage sag (vi)-(x). (c) During voltage swell (xi)-(xv).

power in addition to reactive power requirement of the L_{ext}. The THDs in the load currents are 14.5%, 15.3%, and 13.6% for phases a, b, and c, respectively. After the compensation, the THDs in source currents are reduced to 2.4%, 2.7%, and 2.4%, respectively in phases a, b, and c. The filter and load currents are shown in Figs. 8(iv) and (v), respectively. These waveforms validate the performance of flexible control strategy as 1) source does not exchange reactive power from the system, 2) filter does not supply additional current and reduces system losses, and 3) UPF is maintained at the PCC. These features are not available in conventional DSTATCOM operating in VCM.

Approximate losses in the system are given as follows:

$$P_{loss} = 3\left(I_{f1}^2 R_f + (I_s^{im})^2 R_s + (I_s^{real})^2 R_s\right). \qquad (23)$$

In conventional scheme, the source always exchanges reactive power. Hence, I_s^{im} will be non-zero. Also, this current is supplied by the filter i.e., I_{f1} will be higher. However, in proposed scheme, it is seen that the source does not exchange reactive power in normal operation. Hence, $I_s^{im} = 0$ and I_{f1} is reduced. Hence, proposed scheme reduces losses in the system and utilizes smaller VSI ratings. Small power losses will be there due to the ESR of the external inductor. However, the losses in the ESR will be much smaller than that of reduction of power losses from the conventional DSTATCOM operation.

Voltage sag is created by reducing the source voltage to 0.6 p.u. at t = 0.3 s for 4 cycles. Fig. 8(vi) shows the PCC voltages. Control of reference load voltage based on the coordinated control of fundamental load current, PCC voltage, and voltage across the external inductor allows DSTATCOM to set different constant reference voltage. The proposed scheme detects voltage sag and load voltage is changed to 0.9 p.u. The waveforms of load voltages are shown in Fig. 8(vii). This guarantees continuous, flexible, and robust operation of the load. The source currents are increased during sag period as illustrated in Fig. 8(viii). Fig. 8(ix) shows the filter currents which increase during sag period to support the load voltage. The load currents waveforms presented in Fig. 8(x) are nearly constant during entire operation. Once the sag is removed at t = 0.38 s, slowly all the waveforms reach the pre-sag values. With the results of Figs. 8(vi)-(x), it can be concluded that the proposed scheme makes load operation continuous.

Source voltage is increased to 1.4 p.u. at t = 0.8 s to create swell. The PCC voltages are shown in Fig. 8(xi). The algorithm detects swell and maintains load voltage at 1.1 p.u. The waveforms are shown in Fig. 8(xii). The waveforms of the source, filter, and load currents are shown in Figs. 8(xiii)-(xv), respectively. The filter currents increase during swell which increases the source currents as well. Load currents are nearly constant throughout the operation. Once sag is removed, it is detected by the algorithm and system is brought to the steady state conditions. It confirms effectiveness of the proposed scheme.

VIII. Experimental Results

A reduced scale experimental prototype, as shown in Fig. 9, is developed to validate the capability of proposed scheme. The parameters of the system are given in Table II.

Performance of the DSTATCOM and flexible control strategy at the steady state is shown in Fig. 10(a). The three phase PCC voltages, load voltages, source currents, filter currents, and load currents are shown in Figs. 10(i)-(v), respectively. The scheme makes both three phase source currents as well as load voltages balanced and sinusoidal. The THDs in the

load currents are 18.1%, 17.5%, and 19.4% for phases a, b, and c, respectively. After the compensation, the THDs in source currents are reduced to 3.2%, 3.6%, and 3.4%, in respective phases. Also, source currents are in-phase with the respective PCC voltages. It confirms that the source does not exchange any reactive power with the system. Therefore, the filter currents consist of harmonic and reactive component of load current in addition to reactive current requirement of external inductor.

The performance of the proposed scheme during voltage sag is shown in Fig. 10(b). The PCC voltages shown in Fig. 10(vi) are decreased to 0.6 p.u. during the sag period. The control strategy detects sag and maintains load voltage, as shown in Fig. 10(vii), at 0.9 p.u. during the entire sag period. Moreover, no transient in the load voltage is noticed. It can be observed from Fig. 10(viii) that the source currents are increased during the sag duration. It is due to the fact that the compensator supplies reactive current, as shown in Fig. 10(ix), towards the source to maintain load voltage at a constant value. The load currents are shown in Fig. 10(x). These are drawn as per the load requirement.

Further, PCC voltages are increased to 1.4 p.u. to create voltage swell and corresponding performance waveforms are given in Figs. 10(xi)-(xv). Balanced and sinusoidal load voltages maintained at 1.1 p.u. are shown in Fig. 10(xii). Also, no transient is seen during normal to swell and swell to normal. The source, filter, and load currents are shown in Figs. 10(xiii)-(xv). During swell the filter currents are more which consequently increase the source currents. However, the load currents are nearly same throughout the operation.

IX. Conclusions

This paper has presented design, operation, and control of a DSTATCOM operating in voltage control mode (VCM). After providing a detailed exploration of voltage regulation capability of DSTATCOM under various feeder scenarios, a benchmark design procedure for selecting suitable value of external inductor is proposed. An algorithm is formulated for dynamic reference load voltage magnitude generation. The DSTATCOM has improved voltage regulation capability with a reduced current rating VSI, reduced losses in the VSI and feeder. Also, dynamic reference load voltage generation scheme allows DSTATCOM to set different constant reference voltage during voltage disturbances. Simulation and experimental results validate the effectiveness of the proposed solution. The external inductor is a very simple and cheap solution for improving the voltage regulation, however it remains connected throughout the operation and continuous voltage drop across it occurs. The future work includes operation of this fixed inductor as a controlled reactor so that its effect can be minimized by varying its inductance.

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Chandan Kumar (S'13) received the B.Sc. degree from Muzaffarpur Institute of Technology, Muzaffarpur, India, in 2009; the M.Tech. degree from the National Institute of Technology, Trichy, India, in 2011; and the Ph.D. degree from the Indian Institute of Technology Madras, Chennai, India, in 2014, all in electrical engineering.

He was Institute Postdoctoral fellow at Indian Institute of Technology Madras, Chennai, India in 2014. He worked as Postdoctoral Research Associate with the Chair of Power Electronics, University of Kiel, Kiel, Germany in 2015. He is currently working as assistant professor in electronics and electrical engineering department at Indian Institute of Technology Guwahati, India. His research interests include power electronics application in power system, power quality, and renewable energy.

Mahesh K. Mishra (S'00-M'02-SM'10) received the B.Tech. degree from the College of Technology, Pantnagar, India, in 1991; the M.E. degree from the University of Roorkee, Roorkee, India, in 1993; and the Ph.D. degree from the Indian Institute of Technology, Kanpur, India, in 2002, all in electrical engineering.

He has about 23 years of teaching and research experience. For about ten years, he was with the Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur, India. He is currently a Professor with the Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai, India. His interests are in the areas of power distribution systems, power electronics, microgrids, and renewable energy systems.

Dr. Mahesh is a Life Member of the Indian Society of Technical Education. He is recipient of IETE Prof. Bimal Bose award in year 2015 for his contribution to Power Electronics Application in Power System. He serves as an Editor for the IEEE Transactions on Sustainable Energy.

Marco Liserre (S'00-M'02-SM'07-F13) received the MSc and PhD degree in Electrical Engineering from the Bari Polytechnic, respectively in 1998 and 2002. He has been Associate Professor at Bari Polytechnic and Professor in reliable power electronics at Aalborg University (Denmark). He is currently Full Professor and he holds the Chair of Power Electronics at Christian-Albrechts-University of Kiel (Germany). He has published over 200 technical papers (more than 70 of them in international peer-reviewed journals), 4 chapters of a book and a book (Grid Converters for Photovoltaic and Wind Power Systems, ISBN-10: 0-470-05751-3 IEEE-Wiley, second reprint, also translated in Chinese) with more than 15000 citations. Marco Liserre is listed in ISI Thomson report "The worlds most influential scientific minds" from 2014.

He has been awarded with an ERC Consolidator Grant for an overall budget of 2 MEuro for the project "The Highly Efficient And Reliable smart Transformer (HEART), a new Heart for the Electric Distribution System". He has received the IES 2009 Early Career Award, the IES 2011 Anthony J. Hornfeck Service Award, the 2014 Dr. Bimal Bose Energy Systems Award, the 2011 Industrial Electronics Magazine best paper award and the Third Prize paper award by the Industrial Power Converter Committee at ECCE 2012, 2012. He has been Founder and Editor-in- Chief of the IEEE Industrial Electronics Magazine. Currently, he is Co-Eic of IEEE Transactions on Industrial Informatics. In 2013 he has been elevated to the IEEE fellow grade with the following citation "for contributions to grid connection of renewable energy systems and industrial drives".