Analysis and Control of M3C-Based UPQC for Power Quality Improvement in Medium/High-Voltage Power Grid

Qianming Xu, *Student Member, IEEE*, Fujun Ma, *Member, IEEE*, An Luo, *Senior Member, IEEE*, Zhixing He, *Student Member, IEEE*, and Huagen Xiao

***Abstract*—To enhance the power quality in the medium/high-voltage distribution power systems, a single-phase unified power quality conditioner (UPQC) based on the modular multilevel matrix converter (M3C) is presented in this paper. The M3C-UPQC is comprised of four identical multilevel converter arms and associated filtering inductors. According to the established equivalent circuit of M3C-UPQC, its operation principle and power balance of each arm are analyzed theoretically, and the parameters' design for the arm inductance as well as submodule capacitance is studied. Then, an integrated control method for M3C-UPQC in which the dc circulating current is used to balance the instantaneous active power of each arm is proposed to prevent the capacitor voltages from divergence inter- and intra-arms, so as to achieve voltages balance of M3C-UPQC. Finally, the effectiveness of the proposed control method is verified by a prototype rated at 8 kVA.**

***Index Terms*—Harmonic suppression, modular multilevel matrix converter, reactive power compensation, unified power quality conditioner.**

I. Introduction

In recent years, power quality issues have been drawing more and more attention as a growing number of precision equipments are used. However, with large-scale applications of nonlinear loads as well as mass access of renewable energy generation connected to the distribution systems, such as nonlinear, switching, and reactive devices, a series of power quality problems are arising, for instance, low-power factor (PF), voltage swells or sags, current harmonics [1], [2]. These typical issues are challenges to the voltage and frequency stability associated with reactive and active power. Besides, dispersed generators (DGs), such as the wind power, solar power, and electric vehicle, will play an important role in reducing the burden on the environment in the future distribution systems. In both perspectives, unified power quality conditioners (UPQCs) are highly attractive as they constitute the comprehensive conditioning equipment for improving the power quality and also provide an available interface to connect grid, DGs, and sensitive loads [3]–[5].

A system configuration with series and parallel APFs was first described in [6], in which the APFs were combined to control the integrated power quality problems. In [7], this back-to-back converter structure got engineering application and was named UPQC. After that, many researchers fully investigated both system structures and control methods of the UPQC. A comprehensive overview of UPQC was published for overall understanding in [8]. It is worth noting that there are different topologies for UPQC system, e.g., universal power quality conditioning system [9], UPQC with dispersed generations in the dc-link [10], full-bridge, half-bridge, and three-leg single-phase UPQC [11], interline UPQC [12], and UPQC-based three phase four-wire distribution system [13]. In [14], a soft-switching single-phase UPQC using simple resonant units was proposed, which can improve the efficiency of system. In [15], in order to reduce dc-link voltage rating, a modified three-phase UPQC topology was proposed, which used a capacitor in series with the interfacing inductor of shunt active filter, and the system neutral point was connected to the negative terminal of dc-link capacitor to avoid the fourth-leg requirement of shunt active filter. In [16], a modified UPQC topology without series transformer was studied, which was composed by three back-to-back modules. Each one of them consists in a two-level four-branch topology (connected in shunt with the power grid), together with a single-phase full-bridge topology (connected in series with the power grid). In [17] and [18], an OPEN UPQC was researched which consisted of two controlled shunt and series inverters that have no common dc link. OPEN UPQC has more flexible modularity than traditional UPQC for field applications. In order to manage power quality in distribution network, a multiple-terminal UPQC was presented in [19], which is consisted of one series active filter and multiple shunt-active filters.

There has been a growing interest in modular multilevel converters (MMCs) over the years, which not only effectively reduce the voltage rating of switching devices, but also greatly improve the waveform quality of output voltage [20]–[24]. Apart from their initial target applications related to high-voltage direct-current transmission systems [25], MMCs have been identified as an excellent solution for many other needs. In order to enhance power quality in the medium/high voltage power system, a neutral-point-clamped converter or hybrid-multilevel-converter-based UPQC was researched [26], [27], which provided an effective way for the use of low loss and cost

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Q. Xu, F. Ma, A. Luo, and Z. He are with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail: hnuxqm@foxmail.com; mafujun2004@163.com; an_luo@126.com; 506396463@qq.com).

H. Xiao is with the Hunan University of Science and Technology, Xiangtan 411201, China (e-mail: xiaohuagen@163.com).

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devices. In [28] and [29], a new three-phase ac–dc–ac multilevel UPQC obtained from cascaded three-leg converters was proposed. Such a topology is composed of four three-leg converters in which there are three with single-phase dc links and the fourth one has a three-phase dc link. In [30] and [31], the multilevel three-phase UPQC was presented, and it is composed of single-phase full-bridge cells with well series and parallel assembling. So the power can be evenly divided into each cell to reduce the current and voltage rating of switching devices. In [32], the modular UPQC based on several pairs of H-bridge submodule was investigated for high-power compensation. The H-bridge module in shunt part is connected in series through a multiwinding transformer, and the H-bridge in series part is directly connected in series and inserted in the distribution line. So it can remove the bulky series injection transformer. In [33], in order to improve the harmonic cancellation performance, two types of power cells were adopted for the parallel part of multicell-based UPQC. This topology is assembled using one type of single-phase power cells for compensating disturbances at the fundamental frequency and another type for compensating harmonic currents. In [34], a UPQC based on cascaded multilevel inverter was proposed. The series converter and shunt converter consist of multi-full-bridge submodules, and they were independent of each other. In [35] and [36], a UPQC based on modular multilevel converter (MMC-UPQC) was proposed to apply to medium/high-voltage grid. The series converter or shunt converter consists of 2*N* half-bridge submodules to generate $(2N + 1)$-level output voltages, and they are connected with each other by common dc link. The modular and redundancy design make the converter easily replace fault modules to improve the reliability of MMC-UPQC. So far, the research on UPQC configuration has been focused on the back-to-back inverter. Instead of the multicell-based ac–dc–ac converters with bulky multiwinding transformer and common dc bus, the modular UPQC combined with direct ac–ac converter is likely to provide alternative options in the application of comprehensive power quality improvement. This work is motivated by a context which aims to improve the power quality in the medium/high-voltage distribution power systems by use of ac–ac converters, as well as to analyze the potential problem with same frequency power flows in UPQC applications.

In this paper, a structure of UPQC based on the modular multilevel matrix converter (M3C) is presented, and it can be directly connected to medium/high-voltage power grid for high-power applications. The remainder of this paper is organized as follows: the system structure and equivalent circuit are presented in Section II. Detailed compensation principle and power analysis are shown in Section III. In Section IV, an integrated control strategy is proposed for M3C-UPQC to ensure the submodule capacitor voltage balance. Finally, prototype experiment results in different cases are presented in Section V.

II. System Structure and Equivalent Circuit

A. Topology Structure of M3C-UPQC

UPQC coordinates the series and parallel converters to achieve comprehensive objectives. More precisely, the parallel part of UPQC improves the power factor and restrains the grid current distortion by compensating reactive power and harmonic current components, and the series part compensates the swell, sag, and harmonic distortion of grid voltage to guarantee a well-behaved load power supply.

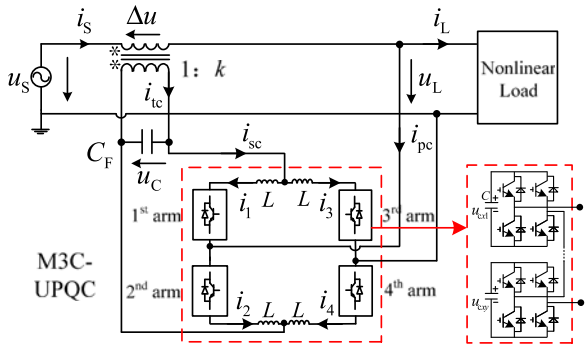


Fig. 1. Schematic of the single-phase M3C-based UPQC.

TABLE I
Comparison of Four Modular UPQCs

Parameter	Modular-UPQC [32]	Modular-UPQC [33]	MMC-UPQC [35]	M3C-UPQC
SIT[1]	NR[2]	R[3]	R	R
PMT[4]	R	R	NR	NR
Switch rated voltage	800 V	800 V	800 V	800 V
Cell number	18	18	144	36
Switch number	144	144	288	144
Capacitor number	18	18	144	36

[1]SIT = Series Injection Transformer; [2]NR = Not Required; [3]R = Required; [4]PMT = Parallel Multi-winding Transformer.

As illustrated in Fig. 1, the grid and sensitive loads are connected to two catercorners of M3C-UPQC, respectively. The single-phase M3C-based UPQC is composed of identical multilevel converter arms and associated filtering inductors. Each arm consists of cascade H-bridge submodules with the number *N*, as shown in the dotted frame. This is not only a strong advantage concerning maintenance aspects, and it also features a very consistent redundancy concept. Additionally, owing to the abundant energy-storage capacitors, slighter dc-link voltages drop/rise of the submodules can be realized during grid voltage sag/swell. Moreover, from [37], it can be seen that the ac/ac MMC with integrated split battery energy storage is potential to be utilized to transfer the necessary active power to the load side even in case of short-time grid faults.

Importantly, this topology of UPQC features identical two-terminal submodules together with their simple and robust interconnections in comparison to other multilevel UPQCs, resulting in a converter structure that enables high availability. Table I shows a brief parameters comparison of four different modular UPQC topologies in a 10-kV system, as illustrated in Fig. 2. The most important parameter, namely the dc-link voltage of each submodule/cell is set as 800 V for a given operating point. The voltage rating of the switch is assumed known as an off-the-shelf switch (Infineon-FF300R12ME4). The following

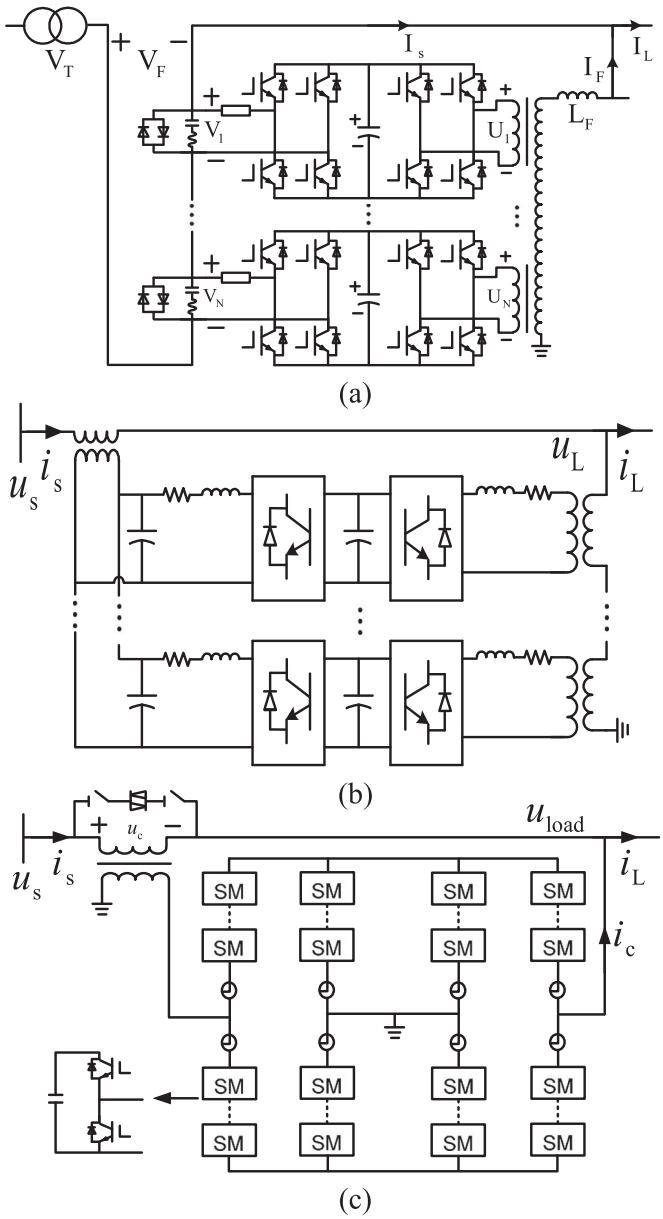


Fig. 2. Three back-to-back modular UPQC topologies. (a) UPQC proposed in [32]. (b) UPQC proposed in [33]. (c) UPQC proposed in [35].

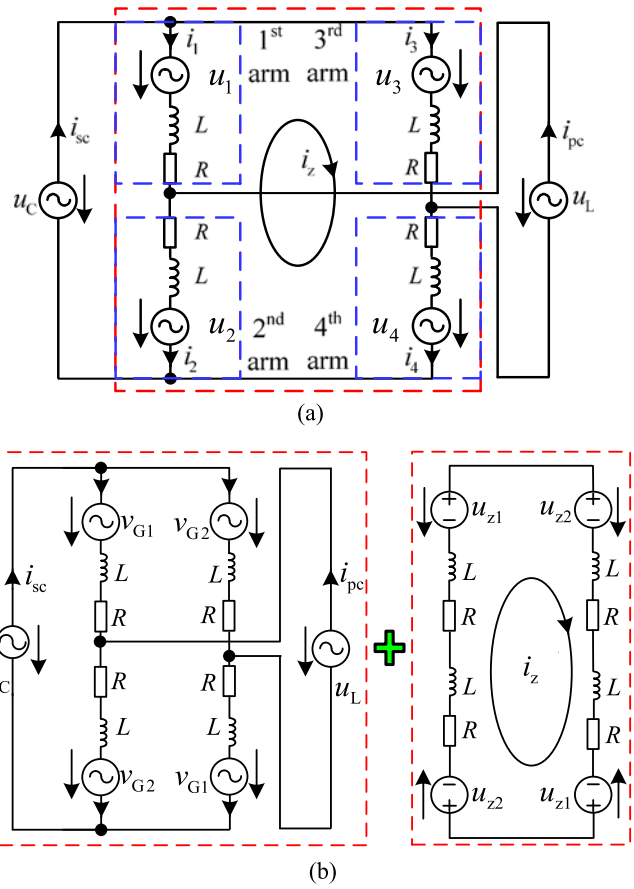


Fig. 3. Controlled voltage-source-based equivalent circuit of M3C-UPQC. (a) Integrated model. (b) Decoupled model.

parameters are adapted in the case of the full modulation and minimum voltage requirement, namely the peak value of rated load voltage. As for the multicell-based UPQCs [32], [33], they need a multiwinding step-down transformer. In order to maintain the dc-link capacitor voltage of each cell stable at 800 V, the minimum cell number is considered as $10 \times 1.414/0.8$, rounding up to 18. Accordingly, the switch number and capacitor number can be obtained. As for the modular back-to-back UPQC [35], without regard to the step-down transformer, the minimum submodule number in one arm is set as $10 \times 1.414/0.8$, namely 18 with rounding up. Consequently, the total number of switches and capacitors are worked out in Table I. Under the same condition, the minimum submodule number in one arm of M3C-UPQC is $10 \times 1.414/0.8/2$, namely 9 with rounding up. And the total number of switches and capacitors can be obtained accordingly.

Apparently, as shown in Table I, it can be seen that M3C-UPQC needs equal power switches but more capacitors compared to multicell-based UPQC. However, it makes the bulky and costly parallel multiwinding transformer and alternating current filter dispensable. It is noteworthy that the UPQC composed of back-to-back MMCs is economically inefficient in comparison with the other topologies in view of twice or more times power switches and capacitors.

B. Equivalent Circuit of M3C-UPQC

According to the structure in Fig. 1, the integrated equivalent model based on controlled voltage source is established as shown in Fig. 3(a), where R and L represent the series resistance and inductance of the filtering inductor, u_x and i_x represent the output voltage and current of the xth arm ($x = 1, 2, 3, 4$), respectively. $i_{\rm sc}$ and $i_{\rm pc}$ are the output current in series side and parallel side of M3C-UPQC, respectively, i_z denotes the circulating current, which only flows inside M3C-UPQC and has no effect on the output current. Generally, the mentioned circulating current should be suppressed as far as possible. However, it also can be used for the voltage balancing control under special conditions. The arm currents are described as (1) in accordance

with Kirchhoff current law

$$\begin{cases} i_{\rm sc} = i_1 + i_3 = i_2 + i_4 \\ i_{\rm pc} = i_2 - i_1 = i_3 - i_4 \\ i_z = (i_4 + i_3 - i_2 - i_1)/4. \end{cases} \tag{1}$$

As described in [22], benefiting from the highly symmetrical structure, the arm current i_x can be expressed as

$$\begin{cases} i_{1,4} = \dfrac{i_{\rm sc} - i_{\rm pc}}{2} \mp i_z \\ i_{2,3} = \dfrac{i_{\rm sc} + i_{\rm pc}}{2} \mp i_z. \end{cases} \tag{2}$$

Subsequently, the direct application of Kirchhoff voltage law results in (3), where u_C is the voltage across the ac filter capacitor C_F and u_L is the load voltage. According to Fig. 3(a), there is

$$\begin{cases} u_1 + u_4 = u_C - u_L - L\dfrac{d(i_1 + i_4)}{dt} - R(i_1 + i_4) \\ u_2 + u_3 = u_C + u_L - L\dfrac{d(i_2 + i_3)}{dt} - R(i_2 + i_3). \end{cases} \tag{3}$$

Assuming u_{z1} and u_{z2} are the injected dc voltages, and v_{G1} and v_{G2} denote the ac components in arm output voltages, so the decoupled ac and dc model of M3C-UPQC can be established as Fig. 3(b). The desired arm voltages are defined by (4), which can be considered as an extension of equations mentioned in [22]. A key element needs to be highlighted that both injected voltages and circulating current are set as dc components, and detailed descriptions will be given in the next section. In consideration of the similarity among four arms, the first arm and fourth arm are paired as group 1, whereas the second arm and third arm are paired as group 2. By doing these, the decoupled model of M3C-UPQC can be obtained

$$\begin{cases} u_{1,4} = v_{G1} \pm u_{z1} = \dfrac{u_C - u_L}{2} - \dfrac{L}{2}\dfrac{d(i_{\rm sc} - i_{\rm pc})}{dt} \\ \qquad -\frac{R}{2}(i_{\rm sc} - i_{\rm pc}) \pm u_{z1} \\ u_{2,3} = v_{G2} \mp u_{z2} = \dfrac{u_C + u_L}{2} - \dfrac{L}{2}\dfrac{d(i_{\rm sc} + i_{\rm pc})}{dt} \\ \qquad -\frac{R}{2}(i_{\rm sc} + i_{\rm pc}) \mp u_{z2}. \end{cases} \tag{4}$$

Besides, according to the voltage loop composed of four arms, the injected voltages should meet

$$u_{z1} - u_{z2} = 2L\frac{di_z}{dt} + 2i_z R. \tag{5}$$

It is important to note the capacitor voltages of all H-bridge submodules in the same arm can be well balanced by use of a proper individual voltage balancing control [38], [39], without affecting the supervisory voltage controls. Hence, the output voltage of each arm can be expressed as (6), where n_x and $u_{{\rm csum}_x}$ are the modulation index and summed capacitor voltages of *x*th arm, respectively. And $n_{\rm xy}$ and $u_{\rm cxy}$ are the individual modulation index and individual capacitor voltage of *y*th submodule, respectively

$$u_x = \sum_{y=1}^{N} n_{\rm xy} u_{\rm cxy} = n_x u_{\rm csum\_x}. \tag{6}$$

Hence, based on (1)–(6), the controllability of the output voltages and currents as well as the circulating current is available by adjusting the modulation index of each arm.

III. Compensation Principle and Power Analysis

A. Operation Principle for External Compensation

As shown in (7), controlling a UPQC involves both stabilized load voltage u_L and sinusoidal grid current i_S, where u_N is the rated voltage with the amplitude of U_N, I_S is the amplitude of grid current, and ω_1 is the fundamental angular frequency. The nonlinear load current i_L can be decomposed into fundamental active current $i_{\rm fd}$, fundamental reactive current $i_{\rm fq}$, and harmonic current i_h, where $I_{\rm fd}, I_{\rm fq}$, and $I_{\rm hi}$ are the respective amplitudes. The indices *m* and *n* in (8) and (9) refer to the maximum harmonic orders in load current and grid voltage, respectively

$$\begin{cases} u_L = u_N = U_N \sin\omega_1 t \\ i_S = i_{\rm pc} + i_L = I_S \sin\omega_1 t \end{cases} \tag{7}$$

$$\begin{aligned} i_L &= i_{\rm fd} + i_{\rm fq} + i_h = I_{\rm fd}\sin\omega_1 t + I_{\rm fq}\cos\omega_1 t \\ &\quad + \sum_{i=2}^{m} I_{\rm hi}\sin\omega_i t. \end{aligned} \tag{8}$$

Some assumptions are made for convenience as follows.

1) The above objectives are achieved irrespective of phase change in the grid voltage as shown in (9), where $u_{\rm Sj}$ is the *j*th harmonic components with amplitude of $U_{\rm Sj}$ and initial phase angle of φ_j as well as the angular frequency of ω_j

$$u_S = U_{S1}\sin\omega_1 t + \sum_{j=2}^{n} U_{\rm Sj}\sin(\omega_j t + \varphi_j). \tag{9}$$

2) The series transformer is ideal and the currents flowing through the ac filter capacitor are disregard, as shown in (10), where *k* is the transformation ratio of transformer, and i_{tc} is the secondary winding current of transformer

$$\begin{cases} u_C = k(u_N - u_S) \\ i_{\rm sc} = i_{tc} = -i_S/k. \end{cases} \tag{10}$$

3) The grid voltage disturbance and load current distortion can be entirely inhibited so that they are pure sinusoidal waveforms. Hence, without regard to the power loss, the generated active power only exists at the fundamental frequency, as shown in (11), where $i_{\rm pcd}$ and $i_{\rm pcq}$ are the transferred active component and compensated components in $i_{\rm pc}$, respectively

$$\begin{cases} i_{\rm pcq} + i_{\rm fq} + i_h = 0 \\ u_L i_{\rm pcd} + u_C i_{\rm sc} = u_L i_{\rm pcd} + k(u_N - u_{S1}) i_{\rm sc} = 0. \end{cases} \tag{11}$$

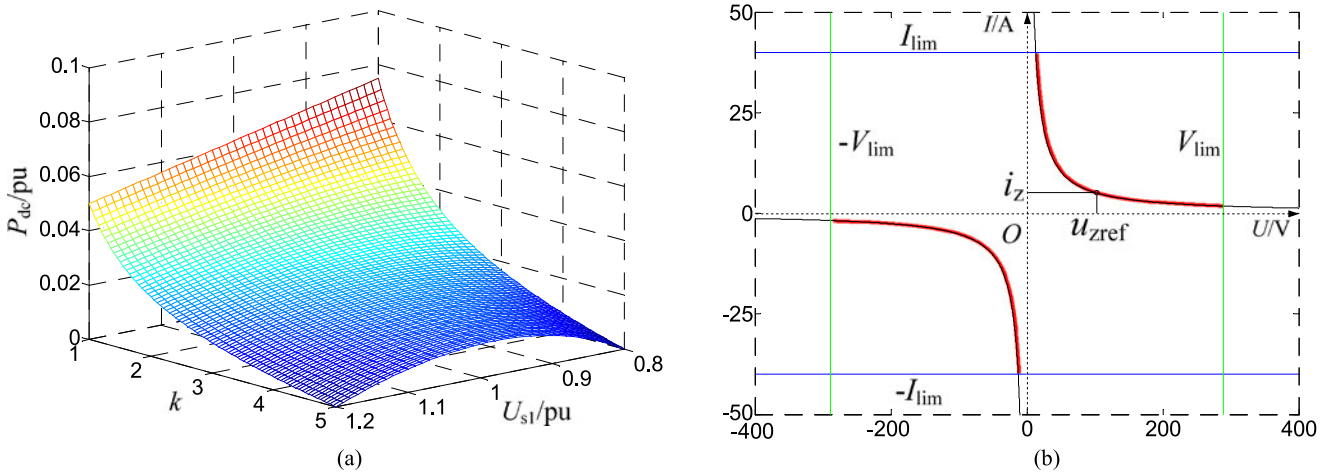


Fig. 4. DC active power analysis. (a) DC active power in dependence of the transformer ratio and grid voltage fundamental component. (b) The limit regions of the injected voltages and current.

Making using of the given definitions in (7), (10), and (11), the equation describing i_S and $i_{\rm pcd}$ can be expressed as

$$\begin{cases} i_S = \dfrac{U_N}{U_{S1}} i_{\rm fd} \\ i_{\rm pcd} = \dfrac{U_N - U_{S1}}{U_{S1}} i_{\rm fd}. \end{cases} \tag{12}$$

Besides, the references of compensating voltage and current can be derived in (13), since the integrals of all the cross product of the voltage and current with different frequencies are zero

$$\begin{cases} u_C^{\rm ref} = k(u_N - u_S) = k(U_N - U_{S1})\sin\omega_1 t \\ \qquad - \sum_{j=2}^{n} kU_{\rm Sj}\sin(\omega_j t + \varphi_j) \\ i_{\rm pc}^{\rm ref} = i_{\rm pcd} + i_{\rm pcq} = \dfrac{U_N - U_{S1}}{U_{S1}} I_{\rm fd}\sin\omega_1 t - I_{\rm fq}\cos\omega_1 t \\ \qquad - \sum_{i=2}^{m} I_{\rm hi}\sin\omega_i t. \end{cases} \tag{13}$$

B. Power Analysis for Arm Groups

According to (5), the internal circulating current is controllable by means of the injected voltages, so the arm power is analyzed in consideration of $i_z \neq 0$. Generally, the arm resistance R and inductance L are relatively small so that their voltage drops can be ignored. Furthermore, it is assumed that the injected voltages and current are decoupled from the output voltages and currents as the injected frequency is different from fundamental frequency. By substituting (7), (10), and (13) into (2) and (4), the instantaneous power of group 1 can be expressed as (14). As a matter of fact, only the components with identical frequencies infer a product whose average value is nonzero. Compared with the fundamental voltage and current components, the relatively small harmonic voltage and current components can be ignored for active power calculation. In addition, due to the fact that the resulting expressions are quite complex, they are not entirely shown. Instead, among the corresponding terms, only the dc components as well as dominating first and second frequency ac components are presented as (14). Same procedures can be adapted to obtain the instantaneous power of group 2, as shown in (15).

As shown by (14) and (15), it is observed that the derived instantaneous power contain active power transfer between two groups mainly caused by the dot product of the voltage and current with fundamental frequency, and its nonzero average value results in capacitor voltages deviation.

Without respect to the injected voltages and circulating current, the dc active power $P_{\rm dc}$ is dependent of both transformer ratio and grid voltage fundamental component. The graph of dc active power $P_{\rm dc}$ plots for the change of the transformer ratio k and grid voltage fundamental component U_{S1} is demonstrated in Fig. 4(a). It can be seen that increasing the values of k results in the increase of $P_{\rm dc}$. The reason is that lower values of k lead to higher forced active current in the secondary winding of series transformer. Besides, it can be found that there is an approximately negative linear correlation between the dc active power $P_{\rm dc}$ and U_{S1} for the smaller value of k. However, this relationship will have one global maximum as a result of higher values of k. Hence, higher transformer ratio is suggested in the case of lower grid voltage fluctuation range

$$\begin{cases} P_{1,4} = u_{1,4} i_{1,4} = \left(\dfrac{u_C - u_L}{2} \pm u_{z1}\right)\left(\dfrac{i_{\rm sc} - i_{\rm pc}}{2} \mp i_z\right) \\ \qquad = P_{\rm dc1,4} + P_{\rm ac1,4} \\ P_{\rm dc1,4} = \dfrac{U_N^2 - k^2(U_N - U_{S1})^2}{8kU_{S1}} I_{\rm fd} - \dfrac{1}{8}\sum_{i=j\geq 2}^{\min(m,n)} kU_{\rm Sj} I_{\rm hi} \\ -u_{z1} i_z \approx \dfrac{U_N^2 - k^2(U_N - U_{S1})^2}{8kU_{S1}} I_{\rm fd} - u_{z1} i_z \\ P_{\rm ac1,4} = \mp\left\{\dfrac{k(U_N - U_{S1}) + U_N}{2kU_{S1}} u_{z1} I_{\rm fd}\sin\omega_1 t \right. \\ \qquad + \dfrac{k(U_N - U_{S1}) - U_N}{2} i_z \sin\omega_1 t - \dfrac{1}{2} u_{z1} I_{\rm fq}\cos\omega_1 t \Big\} \\ \qquad + \left\{\dfrac{k(U_N - U_{S1}) - U_N}{4} I_{\rm fq}\sin 2\omega_1 t \right. \\ \qquad \left. + \dfrac{k^2(U_N - U_{S1})^2 - U_N^2}{8kU_{S1}} I_{\rm fd}\cos 2\omega_1 t \right\} \end{cases} \tag{14}$$

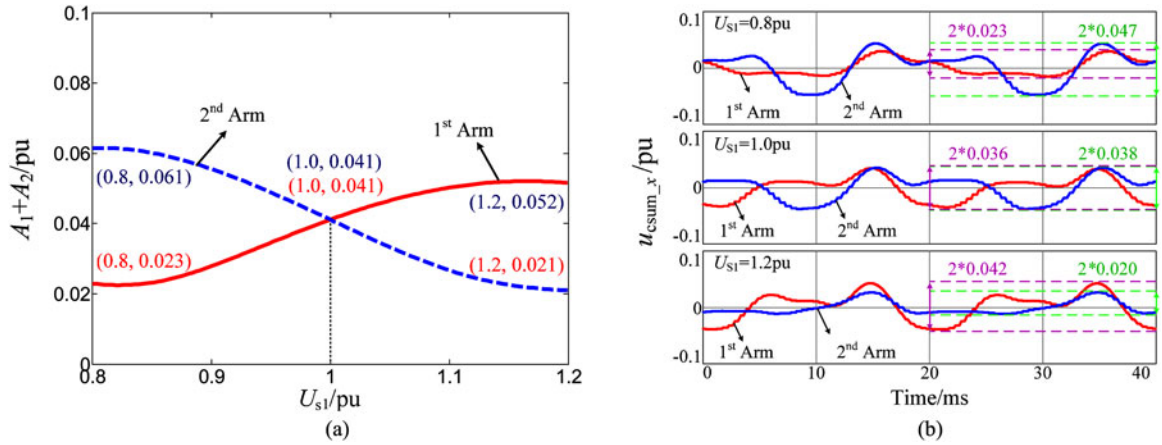


Fig. 5. Analysis and simulation results of the maximum voltage ripple of *x*th arm. (a) Maximum voltage ripple of *x*th arm under different grid voltage fundamental components in theoretical analysis. (b) Simulation results of the summed capacitor voltages of *x*th arm in comprehensive compensation operation with different grid voltage fundamental components (up: $U_{S1} = 0.8$ p.u.; medium: $U_{S1} = 1.0$ p.u.; down: $U_{S1} = 1.2$ p.u.).

$$\begin{cases} P_{2,3} = u_{2,3}i_{2,3} = (\dfrac{u_C + u_L}{2} \mp u_{z2})(\dfrac{i_{\rm sc} + i_{\rm pc}}{2} \mp i_z) \\ \quad = P_{{\rm dc}2,3} + P_{ac2,3} \\ P_{dc2,3} = -\dfrac{U_N^2 - k^2(U_N - U_{S1})^2}{8kU_{S1}} I_{\rm fd} + \dfrac{1}{8}\sum\limits_{i=j\geq 2}^{\min(m,n)} kU_{{\rm S}j} I_{{\rm h}i} \\ \quad + u_{z2}i_z \approx -\dfrac{U_N^2 - k^2(U_N - U_{S1})^2}{8kU_{S1}} I_{\rm fd} + u_{z2}i_z \\ P_{{\rm ac}2,3} = \mp\left\{\dfrac{k(U_N - U_{S1}) - U_N}{2kU_{S1}} u_{z2} I_{\rm fd} \sin\omega_1 t \right. \\ \quad \left. + \dfrac{k(U_N - U_{S1}) + U_N}{2} i_z \sin\omega_1 t - \dfrac{1}{2} u_{z2} I_{\rm fq} \cos\omega_1 t \right\} \\ \quad - \left\{\dfrac{k(U_N - U_{S1}) + U_N}{4} I_{\rm fq} \sin 2\omega_1 t \right. \\ \quad \left. + \dfrac{k^2(U_N - U_{S1})^2 - U_N^2}{8kU_{S1}} I_{\rm fd} \cos 2\omega_1 t \right\}. \end{cases} \tag{15}$$

The capacitor voltages divergence between two groups will appear as a result of unbalanced active power. Consequently, the controllable circulating current and injected voltages inside M3C-UPQC can be used to achieve the active power and capacitor voltages balance of each arm shown as in (14) and (15). It is worth noting that the arm resistances are very small but not zero. Therefore, a minor adjustment Δu_z is superimposed onto the injected voltages to accurately control the internal circulating current according to (5). In (16), $u_{z\rm ref}$ and Δu_z denote the feedforward control output and feedback control output, respectively

$$\begin{cases} u_{z\rm ref} i_z = I_{\rm fd}(U_N^2 - k^2(U_N - U_{S1})^2)/8kU_{S1} \\ u_{z1} = u_{z\rm ref} + \Delta u_z \\ u_{z2} = u_{z\rm ref} - \Delta u_z \end{cases} \tag{16}$$

$$\begin{cases} |(u_C - u_L/2) \pm u_{z\rm ref}| \leq U_{\rm lim} \\ |(u_C + u_L/2) \mp u_{z\rm ref}| \leq U_{\rm lim} \end{cases} \tag{17}$$

$$\begin{cases} |(i_{\rm sc} - i_{\rm pc}/2) \mp i_z| \leq I_{\rm lim} \\ |(i_{\rm sc} + i_{\rm pc}/2) \mp i_z| \leq I_{\rm lim}. \end{cases} \tag{18}$$

It is noteworthy that the injected voltage and current in each arm will not only lessen the total available voltage, but also increase the current stress of switches. As shown in Fig. 4(b), the compromise between injected voltage and circulating current has to be made due to limited capacitor voltage and rated current of submodule according to (17), (18). Moreover, the injected voltages and circulating current can be selected as either the dc components or the ac components with the same frequency. However, the control of dc circulating current is simpler than ac current and will not couple with ac voltages as a result of different frequencies, so it is better to set the injected voltages and current as dc components.

C. Parameters Design of Arm Inductance L and Submodule Capacitance C

As the filtering inductors and submodule capacitors are important components for M3C-UPQC, the design of them is derived as follows. By using the subtraction in (3), irrespective of dc injected voltages and circulating current when designing ac inductor, the following equation can be obtained:

$$L\frac{di_{\rm pc}}{dt} = u_L - e_{\rm pc} - Ri_{\rm pc} \tag{19}$$

where $e_{\rm pc} = u_2 + u_3 - u_1 - u_4/2$. So the arm inductance design of M3C-UPQC can draw on the experience of multilevel inverters [40]. With disregarding the negligible arm resistor *R*, the value of arm inductance *L* is limited as follows:

$$\frac{E_{\rm pc}T_s}{4N\Delta i_{\max}} \leq L \leq \frac{E_{\rm pc} - U_N}{\omega I_{\max}} \tag{20}$$

where $\Delta i_{\max}$ represents the limit value of output current ripples, T_s is the control cycle, $I_{\max}$ denotes the amplitude of output current $i_{\rm pc}$, and $E_{\rm pc}$ is the maximum output voltage in parallel side of M3C-UPQC. According to the designed value range

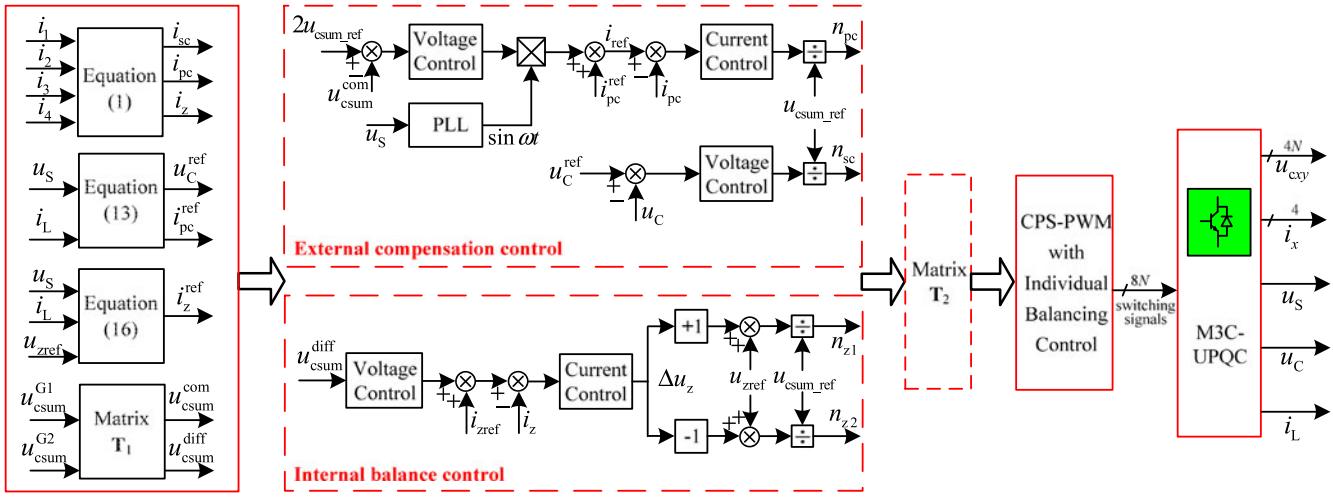
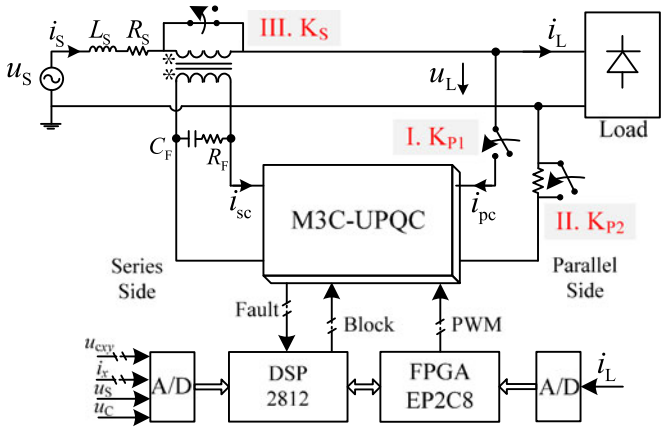
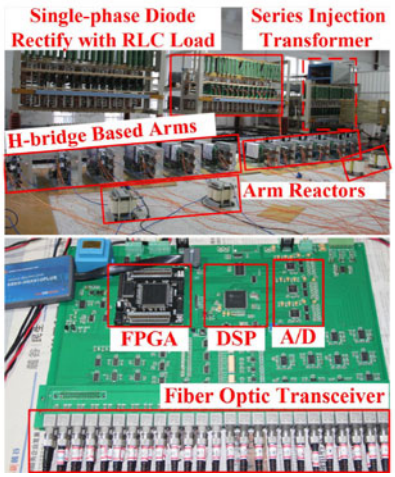


Fig. 6. Block diagram of integrated control for M3C-UPQC.



(a)



(b)

Fig. 7. Experimental setup of M3C-UPQC. (a) Structure diagram of implemented prototype. (b) Photograph of implemented prototype.

TABLE II
SYSTEM PARAMETERS

System Ratings		
Rated apparent power	S	8 kVA
Fundamental frequency	f	50 Hz
Rated load voltage	$U_{L\,\mathrm{rms}}$	220 V
M3C-UPQC Parameters		
Submodule number in per arm	N	3
Arm inductance	L	2 mH
Filter capacitor	C_F	50 μF
Capacitor damping resistor	R_F	2 Ω
Submodules capacitance	C	5 mF
Submodules voltage reference	U_c	100 V
Maximum injected voltage	$u_{z\,\mathrm{ref}}$	60 V
IGBT power modules		FF300R12ME4
IGBT driving modules		2SP0115T2Ax
Load Parameters		
Load resistance	R_L	10 Ω
Load inductance	L_L	5 mH
load capacitance	C_L	1 mF

TABLE III
PARAMETERS OF THE CONTROLLER

Digital signal processor	TMS320F2812
Field programmable gate array	EP2C8Q208C8
Control period	100 μs
Carrier frequency	1 kHz
Kind of PWM	CPS-PWM

of arm inductor, L is selected as 2 mH in the experimental prototype.

Subsequently, assume that the limited value of voltage ripple factor of submodule capacitors is $\zeta_{\max}$. According to (14) and (15), there are dominating first and second frequency voltage ripples in the arm energy. Assume that parameter of power submodules is uniform and their capacitor voltage fluctuations are consistent with each other in the same arm. Hence, the summed capacitor voltages of xth arm can be expressed as $u_{\mathrm{csum}\_x} = u_{\mathrm{csum}\_\mathrm{ref}} + A_1\sin(\omega_1 t + \theta_1) + A_2\sin(2\omega_1 t + \theta_2)$, where $u_{\mathrm{csum}\_\mathrm{ref}}$ is the dc voltage reference, and A_1 and A_2 denote the amplitudes of first and second frequency ripples, respectively. Without regard to the second-order

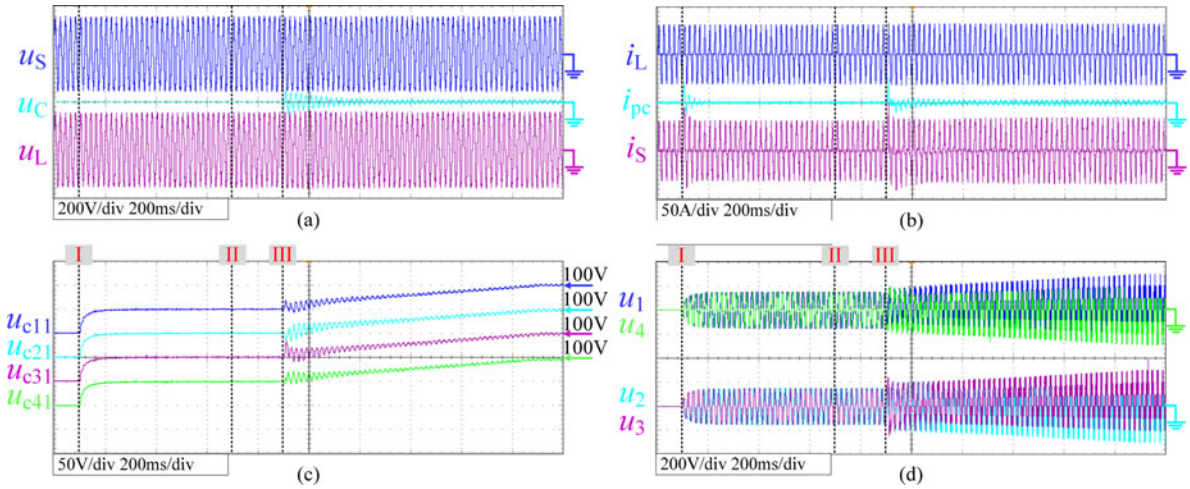


Fig. 8. Startup process. (a) Grid voltage, filter capacitor voltage, and load voltage. (b) Load current, parallel-side current, and grid current. (c) Capacitor voltage of the first submodule in each arm. (d) Multilevel output voltage of each arm.

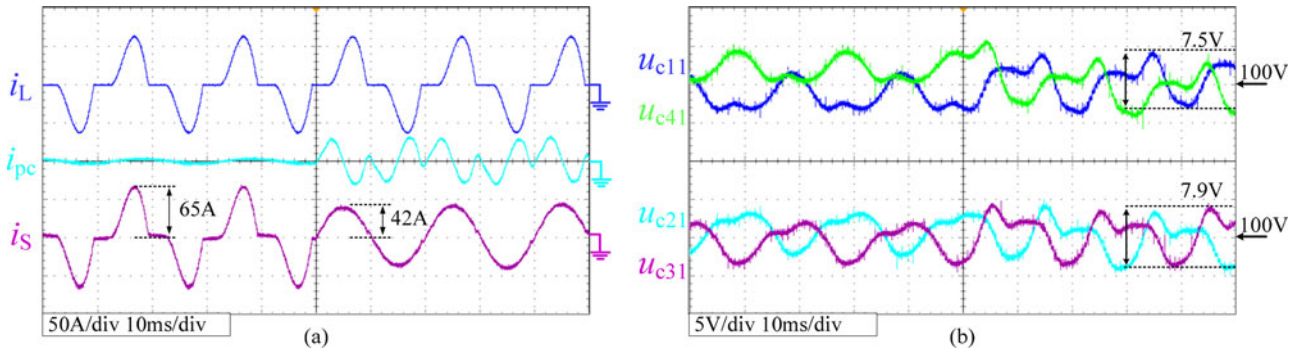


Fig. 9. *CASE A*. (a) Load current, parallel-side current, and grid current. (b) Capacitor voltage of the first submodule in each arm.

terms, the instantaneous power of xth arm can be derived as

$$\begin{aligned} P_{\mathrm{ac}x} &= \frac{C}{2N}\frac{du^2_{\mathrm{csum}\_x}}{dt} = \frac{Cu_{\mathrm{csum}\_x}}{N}\frac{du_{\mathrm{csum}\_x}}{dt} \\ &\approx \frac{Cu_{\mathrm{csum\_ref}}}{N}\{\omega_1 A_1\cos(\omega_1 t+\varphi_1) \\ &\quad +2\omega_1 A_2\cos(2\omega_1 t+\varphi_2)\}. \end{aligned} \tag{21}$$

Recalling the aforementioned expressions for instantaneous power in (14) and (15), the amplitudes of first and second frequency ripples can be obtained as follows:

$$\begin{cases} A_1 = \dfrac{\max\{|NP_{\mathrm{ac}x}(\omega t)|\}}{\omega_1 Cu_{\mathrm{csum\_ref}}} \\ A_2 = \dfrac{\max\{|NP_{\mathrm{ac}x}(2\omega t)|\}}{2\omega_1 Cu_{\mathrm{csum\_ref}}}. \end{cases} \tag{22}$$

Hence, regardless of the phase difference, the maximum ripple of summed capacitor voltages of xth arm can be simplified as A_1+A_2, and it should meet $(A_1+A_2)/u_{\mathrm{csum\_ref}} \le \zeta_{\max}$. As a consequence, the selected submodule capacitance C is limited as

$$C \ge \frac{2\max\{|NP_{\mathrm{ac}x}(\omega t)|\}+\max\{|NP_{\mathrm{ac}x}(2\omega t)|\}}{2\omega\zeta_{\max}u^2_{\mathrm{csum\_ref}}}. \tag{23}$$

Fig. 5 presents the analytic and simulation results of the maximum voltage ripple of xth arm when C is equal to 5 mF. Relationship between the calculated maximum voltage ripple of xth arm and the grid voltage fundamental component in comprehensive compensation operation is illustrated in Fig. 5(a). It can be concluded that the maximum voltage ripples of the first arm and second arm show the approximately opposite variation trend versus the grid voltage fundamental components. The reason for this is that the power flow directions operating at grid voltage swell and swag are contrary. Moreover, there is a global minimum value of the maximum voltage ripples among four arms at the intersection point of two curves, namely $U_{S1}=U_N$. A simulation in a M3C-UPQC under different grid voltage fundamental components is shown in Fig. 5(b). The calculated results are slightly larger than the simulation results since the phase difference as well as harmonic voltages and currents are disregarded. Besides, the ac fluctuations of capacitor voltages in third (fourth) arm are coincident to ac fluctuations of capacitor voltages in second (first) arm but with 180° phase-shifting. Hence, it is practical to design the submodule capacitance by use of (23).

IV. Integrated Control Method

The proposed integrated control strategy is illustrated in Fig. 6. The control problem is split into two subproblems,

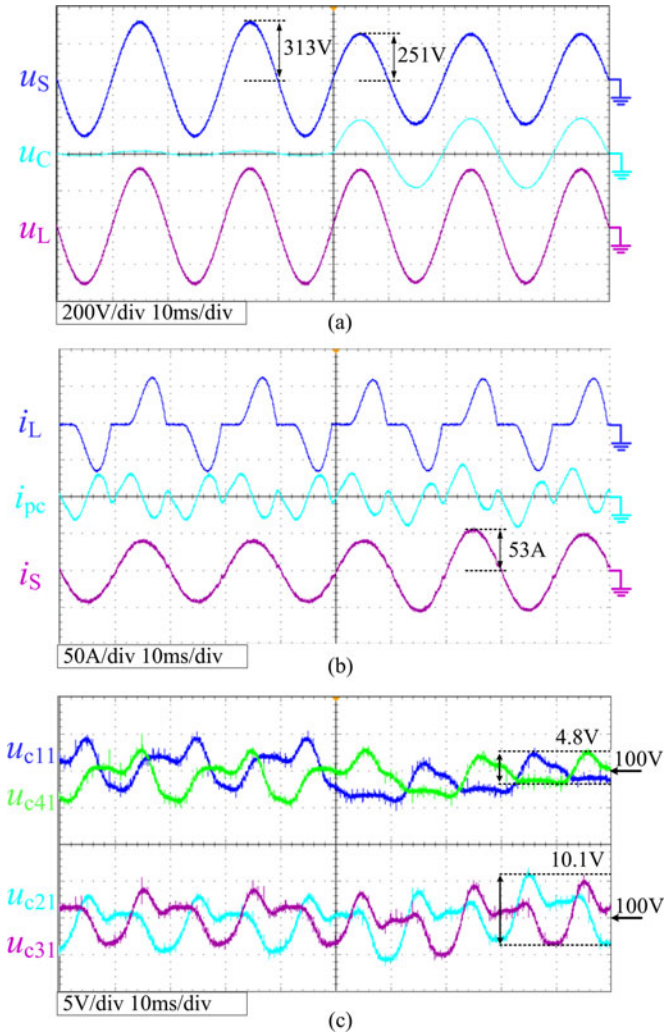


Fig. 10. *CASE B*. (a) Grid voltage, filter capacitor voltage, and load voltage. (b) Load current, parallel-side current, and grid current. (c) Capacitor voltage of the first submodule in each arm.

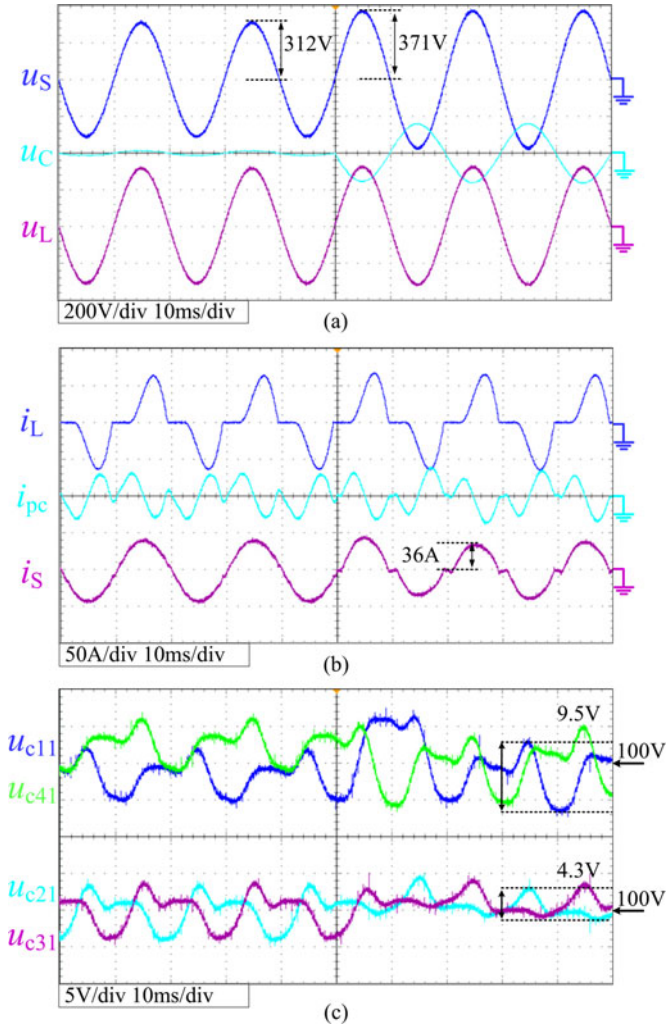


Fig. 11. *CASE C*. (a) Grid voltage, filter capacitor voltage, and load voltage. (b) Load current, parallel-side current, and grid current. (c) Capacitor voltage of the first submodule in each arm.

namely the external compensation control and internal balance control.

A. External Compensation Control

The external compensation control is responsible for the total power stabilization of M3C-UPQC as well as compensation references tracking. Initially, the summed capacitor voltages of group 1 and group 2 can be easily described in (24). The transform matrix $\mathbf{T}_1$ is used to distinguish the common-mode component and differential-mode component, namely $u_{\text{csum}}^{\text{com}}$ and $u_{\text{csum}}^{\text{diff}}$. Moreover, the synchronization requirement with the power grid imposes the need for phase-locked loop (PLL) utilization. So a single-phase second-order generalized-integrator-based PLL [41] is used for the extraction of voltages and currents. Subsequently, a dual-loop control involving the outer common-mode capacitor voltages loop and inner compensating currents loop is implemented as depicted in the dotted frame. More specifically, the voltage control and current control used here are proportional integral (PI) controller and deadbeat controller due to the tolerated track errors. As for the compensation of grid voltage distortion, another PI controller is used as well for reducing the error between the reference value and sampled value across the ac filtered capacitor

$$\begin{cases} u_{\text{csum}}^{G1} = \sum_{y=1}^{N} u_{c1y} + \sum_{y=1}^{N} u_{c4y} \\ u_{\text{csum}}^{G2} = \sum_{y=1}^{N} u_{c2y} + \sum_{y=1}^{N} u_{c3y} \end{cases} \tag{24}$$

$$\begin{bmatrix} u_{\text{csum}}^{\text{com}} \\ u_{\text{csum}}^{\text{diff}} \end{bmatrix} = T_1 \begin{bmatrix} u_{\text{csum}}^{G1} \\ u_{\text{csum}}^{G2} \end{bmatrix} = \begin{bmatrix} 1/2 & 1/2 \\ 1/2 & -1/2 \end{bmatrix} \begin{bmatrix} u_{\text{csum}}^{G1} \\ u_{\text{csum}}^{G2} \end{bmatrix} \tag{25}$$

B. Internal Balance Control

The internal capacitor voltage balancing is encountered in any MMC-based topology. As mentioned, the injected circulating current constitutes an additional degree of freedom to control the differential-mode active power transfers in a decoupled manner. Hence, a dual-loop control involving the outer differential-mode capacitor voltages loop and inner circulating

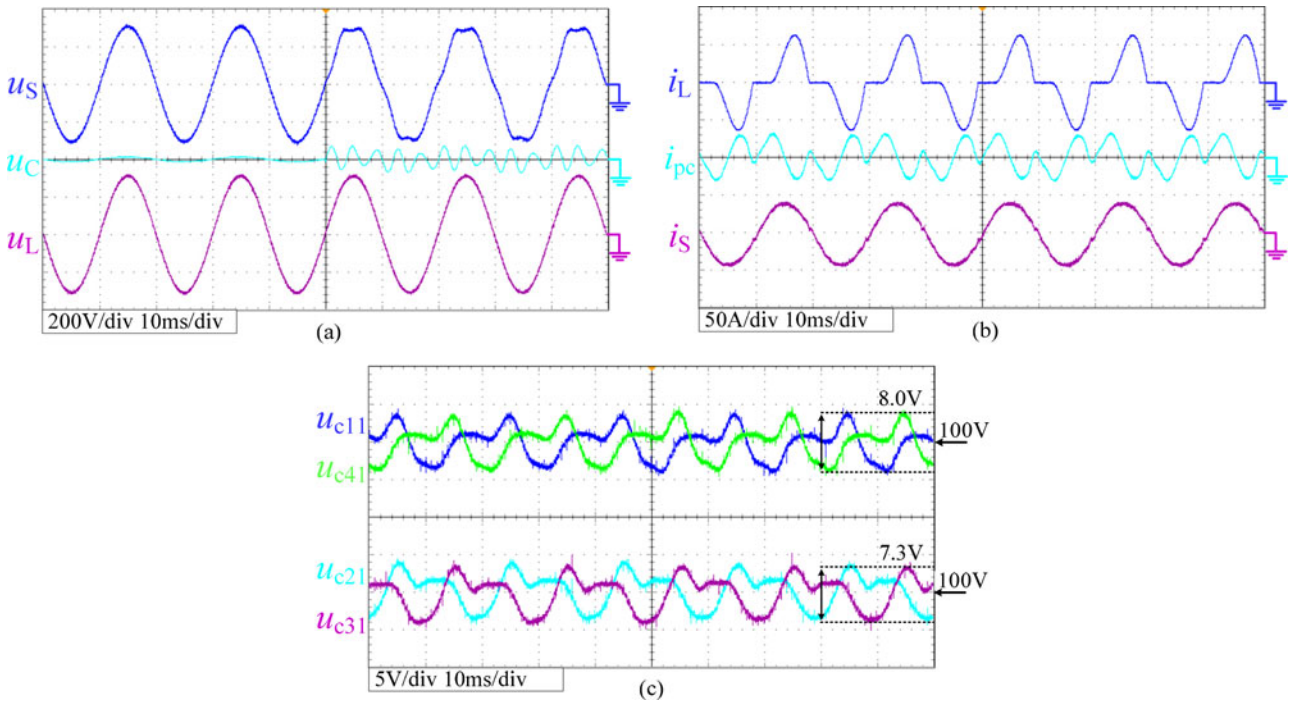


Fig. 12. *CASE D*. (a) Grid voltage, filter capacitor voltage, and load voltage. (b) Load current, parallel-side current, and grid current. (c) Capacitor voltage of the first submodule in each arm.

currents loop is implemented as highlighted in the dotted frame. This is designed to be responsible for redistributing active power between the two arm groups, without affecting the external compensation control. More specifically, two PI controllers are utilized to embody the control of differential-mode capacitor voltages and circulating current in terms of dc components. As known from (17) and (18), the injected voltage and current are selected eclectically with taking overmodulation and overcurrent into account. Given an appropriate injected voltage $u_{z\mathrm{ref}}$, the feedforward signal $i_{z\mathrm{ref}}$ of circulating current can be obtained from (16) to shorten the regulating process in case of grid voltage or load step change. Meanwhile, the differential-mode component of summed capacitor voltages namely $u_{\mathrm{csum}}^{\mathrm{diff}}$ is put into the PI controller for the feedback signal to improve the control precision. Another PI controller is adopted to track the dc circulating current, and its output Δu_z is the feedback correction for $u_{z\mathrm{ref}}$. Then, the injected voltages u_{z1} and u_{z2} can be obtained by adding the feedforward control output $u_{z\mathrm{ref}}$ to the feedback correction Δu_z, as highlighted in the dotted frame.

Finally, making using of the transform matrix $\mathbf{T}_2$, the outputs of aforementioned controllers can be combined to obtain the modulation index of xth arm as shown in (26), which is a direct consequence of (4)

$$\begin{bmatrix} n_1 \\ n_2 \\ n_3 \\ n_4 \end{bmatrix} = \mathbf{T}_2 \begin{bmatrix} n_{\mathrm{pc}} \\ n_{\mathrm{sc}} \\ n_{z1} \\ n_{z2} \end{bmatrix} = \begin{bmatrix} -1 & 1 & 1 & 0 \\ 1 & 1 & 0 & -1 \\ 1 & 1 & 0 & 1 \\ -1 & 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} n_{\mathrm{pc}} \\ n_{\mathrm{sc}} \\ n_{z1} \\ n_{z2} \end{bmatrix}. \quad (26)$$

However, another issue to copy with for M3C-UPQC is the individual voltage balancing control inside the group. This can be achieved by adjusting the calculated submodule duty cycles, so that the supervisory control will remain unaffected. From [38], [39], and [42]–[45], it can be found that quite a few strategies are presented for balancing the individual voltages, so it will be not repeated herein.

V. Experimental Verification

An 8-kVA experimental prototype has been built in order to validate presented structure and proposed control method. Fig. 7(a) and (b) illustrates the system structure and prototype photograph, respectively. It mainly includes four parts: the series injection transformer, M3C-based UPQC, single-phase diode rectifier load, and digital control system based on DSP and FPGA. According to the theoretical analysis in Section III, the transformation ratio of transformer is selected as 1:3 and the maximum injected voltage $u_{z\mathrm{ref}}$ is selected as 60 V. More precisely, it will be changed from 30 to 60 V during the startup process. The fundamental component variation of the grid voltage is generated by a voltage regulator, and harmonic voltages are caused by a high-power harmonic generator. The carrier phase-shifting pulse width modulated (CPS-PWM) method in [38] is adopted for obtaining the driving signals of insulated-gate bipolar transistors (IGBTs). The related parameters are designed according to the specifications of Tables II and III.

The startup process is a key design step of M3C-UPQC due to its series and parallel construction. The precharge circuit mentioned in [1] is used herein. As shown in Fig. 6(a), it mainly includes three steps. 1) The startup process starts when the ac contactor K_{P1} is turned ON, providing the charge of the submodules capacitors through antiparallel diodes. 2) After 600 ms, the ac contactor K_{P2} is turned ON, cutting off the buffer

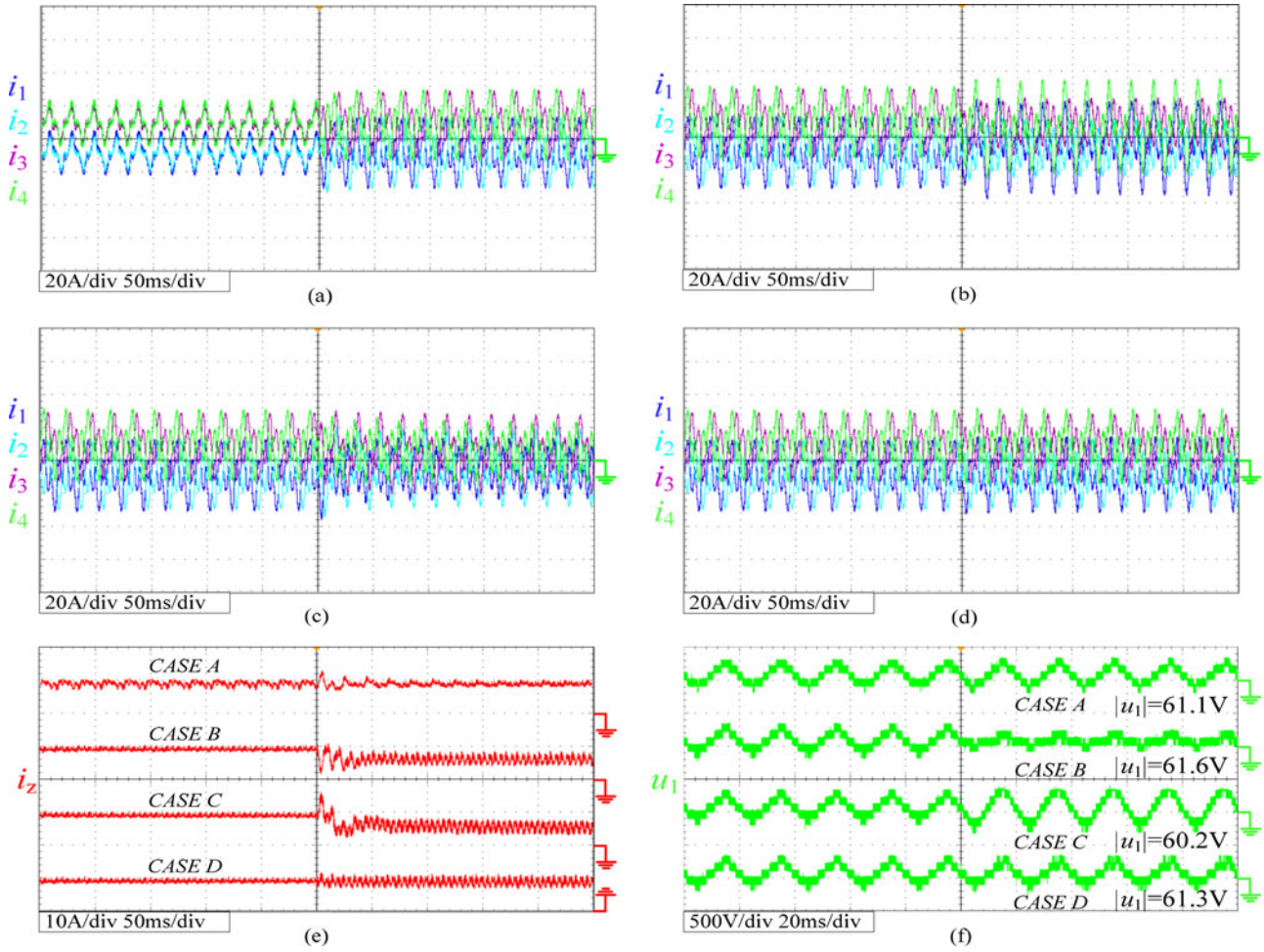


Fig. 13. Arm currents and circulating currents. (a) Reactive compensation and harmonic suppression. (b) Grid voltage sag. (c) Grid voltage swell. (d) Grid voltage harmonic disturbance. (e) Circulating currents in four cases. (f) Output multilevel voltages of first arm in four cases.

resistance. 3) After 100 ms, the ac contactor K_S is turned OFF, inserting the series side. Meanwhile, all the IGBTs are unlocked for the controllable boost process, and it takes about 1000 ms. Fig. 8 illustrates the experimental results during the startup process. It can be seen that the precharge sequence has little impact on the load voltage or load current. Furthermore, the submodule capacitor voltages are gradual during the rise process. Apart from these, other four cases are studied below.

A. Reactive Compensation and Harmonic Suppression

The voltage and current waveforms with reactive compensation and harmonic suppression are demonstrated in Fig. 9. It can be found that the current drained from the grid is sinusoidal with power factors of 0.98. The THD of the load current is 40.21%, while the THD of the grid current is 5.32%, so the reactive and harmonic currents are effectively suppressed by the parallel part of UPQC. Fig. 9(b) reveals the internal characteristics of M3C-UPQC, where u_{cx1} denotes the capacitor voltage of the first submodule in each arm. Apparently, the capacitor voltages in four arms remain at the reference value 100 V. Particularly, the periodic ac fluctuations of submodule capacitor voltages in first arm and second arm are almost the same. The peak-to-peak value of the voltage fluctuation in first arm is 7.5 V and it is 7.9 V in second arm. It can be found that the presented results coincide with Fig. 5 under the rated grid voltage.

B. Grid Voltage Sag

In order to verify the dynamic response of M3C-UPQC, Fig. 10 depicts the experimental results during grid voltage sag, namely 20% of the rated voltage. It is observed that the M3C-UPQC can keep the load voltage at a rated value. Because of the grid voltage sag, the amplitude of grid current increases to 53 A after a fundamental period, and the THD of grid current is 3.86%. Besides, the submodules capacitor voltages keep balance and slight voltage impulse occurs during the grid voltage step. Meanwhile, there are apparent differences among the periodic ac fluctuations of submodule capacitor voltages in first arm and second arm. The peak-to-peak value of the voltage fluctuation in first arm is 4.8 V and it is 10.1 V in second arm. So the results well coincide with Fig. 5 under the grid voltage sag.

C. Grid Voltage Swell

The experimental results during grid voltage swell are illustrated in Fig. 11. It can be seen that the load voltage keeps at

rated value, whereas the amplitude of grid current decreases to 36 A with the incremental THD of 13.9%. Meanwhile, the submodule capacitor voltages keep balance with slight voltage impulse during the grid voltage step. Besides, there are remarkable differences among the periodic ac fluctuations of submodule capacitor voltages in first arm and second arms. The peak-to-peak value of the voltage fluctuation in first arm is 9.5 V and it is 4.3 V in second arm. The results coincide with Fig. 5 as well under the grid voltage swell.

D. Grid Voltage Harmonic Disturbance

In order to evaluate the performance with harmonic disturbance in the grid voltage, a high-power harmonic generator is used to inject fifth and seventh harmonic voltages. From Fig. 12, it can be found that the THD of the grid voltage is equal to 6.96%, while the load voltage has THD equal to 1.57%. The THD of the grid current remains almost the same, namely 5.40%. So the harmonic voltages are effectively compensated by the series part of UPQC. The capacitor voltages in four arms remain well balanced and show little changes compared with *CASE A*. Hence, it proves that ignoring the harmonic voltages and currents has little influence on the instantaneous power calculation.

Fig. 13(a)–(d) shows the arm current waveforms in four cases. It can be seen that the arm currents are limited to 40 A even during the pulsed current process. Moreover, the circulating currents waveforms during four cases are depicted in Fig. 13(e). The circulating current in *CASE A* is 8.93 A, and it is slightly higher than the analytic result calculated from (16), namely 8.81 A. In *CASE B*, the circulating current decreases to 5.81 A, which approximates equal to the analytic result, namely 6.27 A. It can be found that the circulating current decreases further to 5.23 A, which is slightly higher than the analytic result of 4.92 A. In *CASE D*, the circulating current with harmonic voltages compensation slightly reduces to 8.67 A due to the active power generated by the harmonic voltage and current components. It can be concluded that the circulating currents show small overshoots even during the step of grid voltage or compensated current. Fig. 13(f) illustrates the output multilevel voltages of first arm in four cases. It can be seen that the injected dc voltages in four cases are 61.1, 61.6, 60.2, and 61.3 V, respectively.

VI. Conclusion

A single-phase UPQC configuration based on single-phase M3C has been studied in this paper. The assembling of unified modules makes it possible to use low-voltage power devices according to an adequate number of submodules, which allows the use at medium/high-voltage grid. The intermediate dc line in the back-to-back converters is avoidable, which is beneficial to simplify the encapsulation of the overall system. In addition, an integrated control strategy is proposed to balance the power distribution among different H-bridge arms based on special features of M3C-UPQC. The operation of the M3C-UPQC is confirmed through a downscaled experimental prototype.

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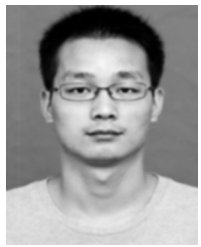

Qianming Xu (S'15) was born in Henan, China, 1989. He received the B.S. degree from the College of Electrical and Information Engineering, Hunan University, Changsha, China, in 2012, where he is currently working toward the Ph.D. degree.

His research interests include multilevel converters, power quality control, electric drive, and power conversion control.

Fujun Ma (M'15) was born in Hunan, China, 1985. He received the B.S. and Ph.D. degrees from Hunan University, Changsha, China, in 2008 and 2015, respectively.

Since 2013, he has been an Assistant Professor with the College of Electrical and Information Engineering, Hunan University. His research interests include power quality managing technique of electrified railway, electric power saving, reactive power compensation, and active power filters.

An Luo (A'09–M'09–SM'09) was born in Changsha, China, 1957. He received the B.S. and M.S. degrees from Hunan University, Changsha, China, in 1982 and 1986, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1993.

He was a Professor with the Central South University between 1996 and 2002. Starting in 2003, he became a Professor at Hunan University. He is involved in research on power conversion system, harmonics suppression and reactive power compensation, and electric power saving.

He has published more than 100 journal and conference articles.

Dr. Luo serves as the Associate Board Chairperson of the Hunan Society of Electrical Engineering. He also serves as the Chief of the Hunan Electric Science and Application Laboratory.

Zhixing He (S'15) was born in Hunan, China, 1989. He received the B.S. degree from the College of Information Science and Engineering, Central South University, Changsha, China, in 2011. He is currently working toward the Ph.D. degree in the College of Electrical and Information Engineering, Hunan University, Changsha.

His research interests include model predictive control, static var compensator, and modular multilevel converter.

Huagen Xiao was born in Hunan, China, 1979. He received the B.S. and M.S. degrees from the Changsha University of Science and Technology, Changsha, China, in 2005 and 2011, respectively, and the Ph.D. degree from Hunan University, Changsha, in 2015.

Since 2015, he has been a Lecturer with the Hunan University of Science and Technology, Xiangtan, China. His research interests include power electronics, harmonics suppression, reactive power compensation, and microgrid.