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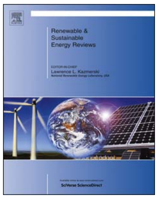

Active power filter (APF) for mitigation of power quality issues in grid integration of wind and photovoltaic energy conversion system

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ABSTRACT

The deep integration of renewable energy resources, including solar photovoltaic (PV) and wind turbine (WT) energy, mainly depend on the inexpensive technological improvement of global emissions and the precise techniques for power quality. Grid-connected inverters act as key components in distributed generation systems for cutting-edge technology. The inverter connects the renewable energy sources and power distribution network systems for the conversion of power. In grid-connected systems, several current and voltage harmonics affect the system performances. Likewise, highly unstable devices coupled with the growing demand for nonlinear loads and renewable energy resources influence the power networks and systems performance in terms of power quality. The effective solutions to these problems are passive filters (PFs), static var generators, and active power filters (APFs). However, the use of PFs in a high-power system increases its cost, size, and weight. This study aims to assess the most advanced APFs by reducing the number of power switches and focus on the reduction of cost, size, and weight of grid-connected inverters. Several studies compared and evaluated reduced-switch-count APF inverter topologies, such as AC–AC, back-to-back, and common leg, under the single-phase and three-phase systems. Recently, cost-effective solutions to reduce the number of components, transformerless inverters, multilevel and multifunctional inverters based on the APF in PV, and wind energy conversion systems have been greatly explored. The current techniques and their limitations for developing advanced inverter-based devices for renewable energy systems are discussed with justifications. Therefore, this review would potentially help industrial researchers improve power quality in PV and WT energies and power distribution network systems.

1. Introduction

The demand for electricity in the modern industrial world is rapidly increasing, from household utilities to commercial industries. Integration of distributed energy resources (DER) [1], such as solar photovoltaic (PV) systems [2], wind energy conversion system (WECS) [3], fuel cells [4], distributed power generation systems (DPGSs) [5], and storage devices [6], improves the reliability and electric power quality while decreasing the loss of power distribution or transmission networks. PV and wind power are the two leading renewable energies resources for reducing the continuous burden on the national power grid and the global environment.

In the power utilization industry, an increasing number of renewable energy devices, as well as linear and nonlinear loads, are being introduced; these devices include the nonlinear rectifier and static var compensator (SVC), which affect daily life [7]. Integrated grid PV and wind energy systems produce certain harmonics, heat, and other complicated power-quality issues, thereby affecting the supply current and voltage sinusoidal waveform spectra [8] in terms of lower system efficiency, overheating of transformers, increased malfunction of motors and cables, increased power loss, necessity of protection devices [9], and the limited life period of wind turbine generator [10] and solar PV modules [11]. The power output is stochastic and the energy resource is intermittent. Therefore, proper current harmonic and power-quality mitigation methods are required to enhance the reliability of the renewable grid-connected system. Various solutions have been proposed to solve the power-quality issues [12], such as unbalanced systems, load balance, injected harmonics, excessive neutral current, reactive power burden, and the network interference in electrical systems. Filters are traditionally used in grid-integrated systems in combination with passive filters (PFs) [13] against series harmonics. As such, PFs have limited use because of issues, including limited filtering, specific load ranges, fixed compensation, larger sizes, parallel and series negative resonance between grids, and filter

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Nomenclature

v_s	(a, b, c) three-phase source voltage
i_s	(a, b, c) three-phase instantaneous source current
i_L	(a, b, c) three-phase load current
i_F	(a, b, c) three-phase filter compensator current
C_f	Capacitor filter
L_f	Inductor filter
L_s	Source-side inductor
L_{AC}	Load-side inductor
V_{dc}	DC-link voltage
C_{dc}	DC-link capacitor
DER	Distributed energy resources
PV	Photo voltaic
WECS	Wind energy conversion system
DPGS	Distributed power generation system
PQ	Power quality
WT	Wind turbines
WTG	Wind turbine generator
DVR	Dynamic voltage regulator
ML-MFI	Multilevel multifunctional inverter
VOC	Voltage oriented control
GHG	Greenhouse gasses
RE	Renewable energy
PWM	pulse width modulation
SPWM	Sinusoidal pulse width modulation
SAPF	shunt active power filter
HAPF	Hybrid active power filter
PF	Passive filter
VSC	Voltage Source Converter
THD	Total Harmonic Distortion
SRF	synchronous-reference-frame
PLL	phase locked loop
UPS	uninterruptible power supply
PCC	point of common coupling
FF	Feed-forward
FB	Feed-back
AC	Alternating current
DC	Direct current
PI	Proportional Integral
P/Q	Active and Reactive Power
EMI	Electromagnetic interference
SiC	silicon carbide
SBD	Schottky barrier diode
USMC	Ultra-sparse matrix converter
ZVS	Zero voltage switching
ZVT	Zero voltage transition
ZCT	Zero current transition
CMV	Common-mode voltage
CMC	Conventional matrix converter
PMGS	Permanent magnet synchronous generator
DFIG	Doubly fed induction generator
ULTC	Under Load Tap Changer (ULTC) transformer
HERIC	High efficient and reliable inverter concept
UPQC	Unified power quality conditioner
DSTATCOM	Distributed static synchronous compensators
STATCOM	Static synchronous compensators
SVC	Static var compensator
SVG	Static var generator
DVR	Dynamic voltage restorer,
OLTC	On-load tap changer,
AVC	Automatic voltage control,
SDBR	Series dynamic breaking resistor,
TCSC	Thyristor controlled series capacitor
UPFC	Thyristor controlled series capacitor.

impedance [14–17]; these issues cause the rapid decay of passive components [18].

According to surveys of grid-integrated systems, such as PV inverters [19] and wind energy systems [20], the power-quality issues are addressed by the use of more advanced filtering technologies, such as a static synchronous compensator, active power filter (APF), dynamic voltage regulator, multilevel inverter, power-monitoring system, and unified power quality conditioner (UPQC). However, the shunt APF (SAPF) is the most dominant and liberal solution against problems of power quality, with reactive power and current harmonics compensation [21–24]. The filter performance depends on inverter parameters, control schemes, and reference current detection techniques [25]. A reference current signal is extracted by harmonic load detection techniques, such as the instantaneous power theory (p–q theory), fundamental positive sequence methods, and synchronous detection [26], for effective control of the APFs.

Two international standards, IEEE-519 [27,28] and IEC 61000-3-2 [29], provide a boundary for all power utility companies in the design and operation of their systems. With the increasing load demand, the APF rating [30] also increases with the accumulating system capacity and cost. As a solution, hybrid APFs (HAPF) are used to configure the PF with SAPF [31]. In HAPF operation, both filters are controlled, such that the low-order harmonics are eliminated by SAPF operation [32], whereas the higher frequency harmonics are canceled by PF. APFs reduce the load current disturbances, which improve current and voltage harmonic compensation. Fig. 1 illustrates the hierarchical structure of renewable energy with power sources and energy storage resources in a power distribution network [33–36].

Recently, several HAPF topologies use transformers and an excessive number of passive components as key tools to manage the filter size, cost, and weight optimization. However, the transformerless topologies achieve a safer and higher system efficiency, smaller volumetric size, cheaper cost, and more compact structures as compared with older transformer-based topologies. The elimination of a transformer generates several problems, including efficiency degradation, safety complications, leakage current, and the installation of a

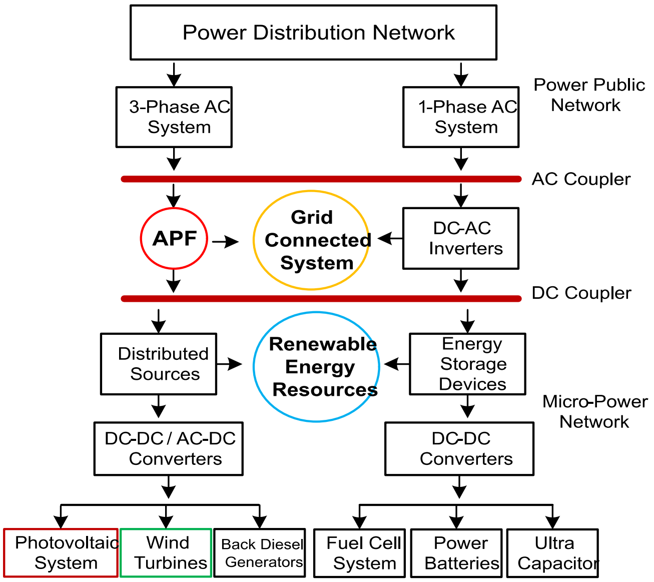

Fig. 1. Hierarchical structure of renewable power sources and grid-connected inverters in a power distribution network.

Table 1
Comparison of different transformerless PV inverter topologies.

	H-bridge (unipolar PWM)	H-bridge (bipolar PWM)	Half-bridge	HERIC topology	H5 Topology	Half-bridge with GCC	Cascaded H-bridge (*n*cells)	NPC half-bridge	Flying capacitor (FC)	NPC variant	Conergy NPC	Active NPC (ANPC)
Input capacitors	1	1	2	1	1	2	η	2	3	4	2	2
Input capacitance	Low	Low	High	Low	Low	Medium	Highest	High	High	High	High	High
Switches	4	4	2	6	5	4	4η	4	4	4	4	6
Diodes	0	0	0	2	0	0	0	2	0	2	0	0
Transistor voltage	400 V	400 V	800 V	400 V	400 V	800 V	$400\ \mathrm{V}/\eta$	400 V	400 V	400 V	400 V	400 V
Output voltage level	3	2	2	3	3	2	$2\eta - 1$	3	3	3	3	3
First harmonic	2FSW	FSW	FSW	2FSW	2FW	FSW	2ηFSW	2FSW	2FSW	2FSW	2FSW	2FSW
EMF interference	Low	High	High	Low	Low	High	Very Low	Low	Low	Low	Low	Low
No. of MPPTs	1	1	1	1	1	2	η	1	1	1	1	1
Leakage current	High	Low	Lowest	Lowest	Lowest	Lowest	Medium	Lowest	Lowest	Lowest	Lowest	Lowest

resonant circuit. Different power converter combinations shunted at the point of common coupling work as an interface between the utility and renewable energy source, depending on the topology structure and modulation scheme. However, the fluctuating common mode voltage and the absence of leakage current in the PV grid-connected system contribute toward the improvement of the system voltage and frequency as compared with traditional topologies. A brief comparison of different transformerless PV inverter topologies is presented in Table 1[37–41]. The total system cost is compares in terms of the switch count and system efficiency [33] with three issues: the galvanic connection, grid voltage fluctuation to ground at input poles, and safety [37,42].

Electrical transmission system and loads operate on the AC grid power [43], whereas the output voltage of renewable energy sources operates on direct current (DC) power. For stand-alone and grid-connected systems, an inverter is the key device required to convert AC power to DC power. The inverter is mounted from the low-power KW range to the higher-power MW range [44] to construct the output AC sinusoidal waveform, which is accomplish by the series or parallel combination of electronic switch devices [45]. Developments in the large-scale PV power system and wind generation systems subject inverters to continuous evolution and make these inverters indispensable. Despite the increasing demand, a major issue of inverters is the larger amount of power switching components, such as insulated gate bipolar transistors (IGBTs) and metal-oxide semiconductor field effect transistors (MOSFETs). Several pure SAPFs are limited by the use of high-power-rating components to improve the utility power factor correction and current harmonic compensation. When connected to the electrical grid, the increased number of semiconductor switch components produces higher switch losses, which contributes to harmonics in the output voltage waveform, degrades the system efficiency [46], and causes the overall system performance to deteriorate [47]. Recently, a reduced switch count has become a cutting-edge solution in power electronics technology, including power semiconductor devices, power conversion circuits, sensors, and control circuits. Despite the importance of component reduction for advancing energy issues, literature on the reduction of switches in APFs is limited.

This in-depth review presents the advances in switch reduction of APFs and focuses on the cost, size, and weight reduction of grid-connected inverters. This paper provides a broad and in-depth literature review to the researchers in the field of reducing devices and grid-connected PV and wind turbine (WT) energy conversion systems. Some potential research topics are also included; the reduction of components, transformerless inverters, and multilevel multi-functional inverters (ML-MFI) for APFs in the PV and WECS are discussed. Different topologies, including single-phase and three-phase system classes, are presented, compared with other topologies, and evaluated based on the total harmonic distortion (THD), harmonic mitigation, the active and reactive power compensation, component ratings, advantages, and disadvantages. The review provides a benchmark for the further development and exploration of other switch reduction techniques that have received little attention from researchers. This paper is divided into six sections, starting with a brief introduction in Section 1. Section 2 provides a brief description of the grid-connected structure of the PV and WECS, with emphasis on the power quality issues. Section 3 illustrates the basic classification and recent advances in SAPF topologies, as well as their main characteristics. In Section 4, the performance of these topologies is discussed, evaluated and analyzed. The SAPF technologies are also briefly compared. Potential further research work is described in Section 5, with concluding remarks in Section 6.

Table 2
Comparison of APFs in grid-inverter topologies.

Ref	Topology	Modulation/ control	Capacity	Switching frequency (kHz)	No. of switches	Trans-former	No. of diodes	No. of DC capacitors	THD (%)	PV/DC-link voltage	Grid-connected functions
Single-phase System											
[63]	Full bridge	SPWM/PI	≤1.5 kVA	20	4	0	2	1@1000uF	3.09	–	PV-APF
[53]	Full bridge	Hysteresis	1 kVA	14.2	4	1	0	1@-	2.31	150 V	PV-APF
[64]	Full bridge	SPWM/PI	≤1.5 kVA	20	2	0	2	1@940μF	4.5	250 V	PV-APF
[65]	Full bridge	SPWM/PI	3 kVA	–	4	1	0	–	< 5	246 V	PV-APF
[66]	Full bridge	SPWM/Lyapunov	–	10	4	0	0	–	< 5	100 V	PV-APF
[67]	Full bridge	SPWM/PI	≤1 kVA	–	4	0	1	1@200uF	–	14 V	PV-APF
[68]	Full bridge	SPWM/repetitive	4 kVA	10	4	0	0	1@2.2mF	2	400 V	PV-APF
[69]	Full bridge	SPWM/PI	1 kVA	–	4	0	0	–	–	–	PV-APF
[70]	Three leg	SPWM/PI	1 kVA	18	6	0	1	1@1000uF	3.19	17 V	PV-APF
[71]	HB ZVS	SPWM/PI	1 kVA	100/10	6	–	–	–	–	–	PV-APF
Three-phase System											
[72]	H-bridge	SPWM/PI	1.1 kVA	20	6	0	2	1@2200 pF	7.8	400 V	PV-APF
[73]	H-bridge	SPWM/PI	10 kVA	–	6	0	0	–	–	–	PV-APF
[74]	H-bridge	Hysteresis	150 kVA	–	6	1	0	1@5uF	1.29	800 V	PV-APF
[75]	H-bridge	SPWM/FLC, PI	–	–	6	1	0	0	2.5	500 V	PV-APF
[76]	H-bridge	SPWM/FLC, PI	20 kVA	–	12	1	0	–	–	–	PV-APF
[77]	ZVI	SPWM/FLC, PI	7.5 kVA	–	6	0	1	2@1500uF	4.21	100 V–60 V	PV-APF
[61]	3 L- NPC	SPWM/FLC, PI	1 kVA	–	14	0	3	2@3mF	–	1100 V	PV-APF
[78]	Four bridge	3D-SVPWM	–	10	8	0	0	1@850uF	13	350 V	PV-APF
[79]	Full bridge	Hysteresis/LQR	–	–	12	1	0	1@-	< 0.5	3.5 kV	PV-APF
[80]	H-bridge	SPWM/FLC, PI	30 kVA	10	12	1	0	2@6600uF	–	700 V	PV-APF

2. Mitigation of power quality and distributed generation systems

2.1. Grid-connected APF-PV inverter

As discussed above, the main aim of installing the PV system at the PCC [48,49] is to improve the operation of power distribution systems and to generate active power. However, to prevent the additional cost of the power circuit, several PV-fed grid interactive topologies combined the PV inverter with the additional functionality of SAPF [50], as well as voltage and reactive power support. The PV inverter injects the compensating current into the grid to filter the load current harmonics [51–53]. In addition, the inverter uses the active power produced from the PV solar energy system. On the other hand, the APF are introduced in the PV system [54,55] to improve the power conversion efficiency, reliability, and current harmonic distortions of the system.

Recently, the ML-MFI has become the most dominant technology used in the PV grid-integrated electrical power generation systems. At high DC-rated voltage, it produces the output waveform in steps with low harmonic distortion waveform. It easily controls multifunctional inverter issues such as grid current harmonic and unbalance mitigation, reactive power compensation, control voltage at PCC [56,57] and transient process in between the PV generator to utility grid during the APF operation. The ML-MFI topologies are installed in high-rated and large PV systems because of its advantages, such as low harmonic and power dissipation and low electromagnetic interference (EMI) outputs. Table 2 summarizes the comparison between the grid-integrated PV inverter topologies [58–60] and the additional functionalities of APFs. In Refs. [61,62], a three-level NPC-MFGCI PV system is controlled more efficiently with a modified voltage-oriented control and space vector PWM (SVPWM) technique to provide shunt active filtering, reactive power compensation, and load current balance to the utility grid.

SAPF can integrate with the PV grid-connected system for harmonic elimination content and reactive power compensation [81] to keep the DC-link voltage constant. A precise mathematical model is needed [82] for the controllers, thereby making the controllers more independent from parameter variation. By contrast, energy storage systems, such as batteries, super capacitors, and flywheels, are programmed to overcome the intermittency problem in renewable PV energy systems. The inherent characteristics of the PV systems decreased the power generation to 15% per second, thereby affecting the performance of the grid network. Therefore, the energy storage systems maintain the constant voltage [83] by reducing voltage fluctuation [84] and maintaining higher PV efficiency [85]. PV systems also help to suppress the harmonic content and regulate the compensating reactive power, thereby enhancing the reliability of the PV grid-integrated system [86].

Table 3
Control parameters affected by the reactive power-compensating devices.

Parameters	OLTC	Capacitor & Reactor Bank	AVC	DVR	SDBR	STATCOM	SVC	TCSC	UPFC
Reactive power	*	***	**			****	***	**	****
Active power	*	**	**	**	**	*	*	**	
Voltage stability	*	**	**			****	***	***	****
Voltage	*	**	**			****	***	**	****
Flicker		*				****	***		****
Harmonic reduction		*							****
Power flow								***	****
Oscillation damping		*		**	***	***	**	***	****

High number of “*” is preferred

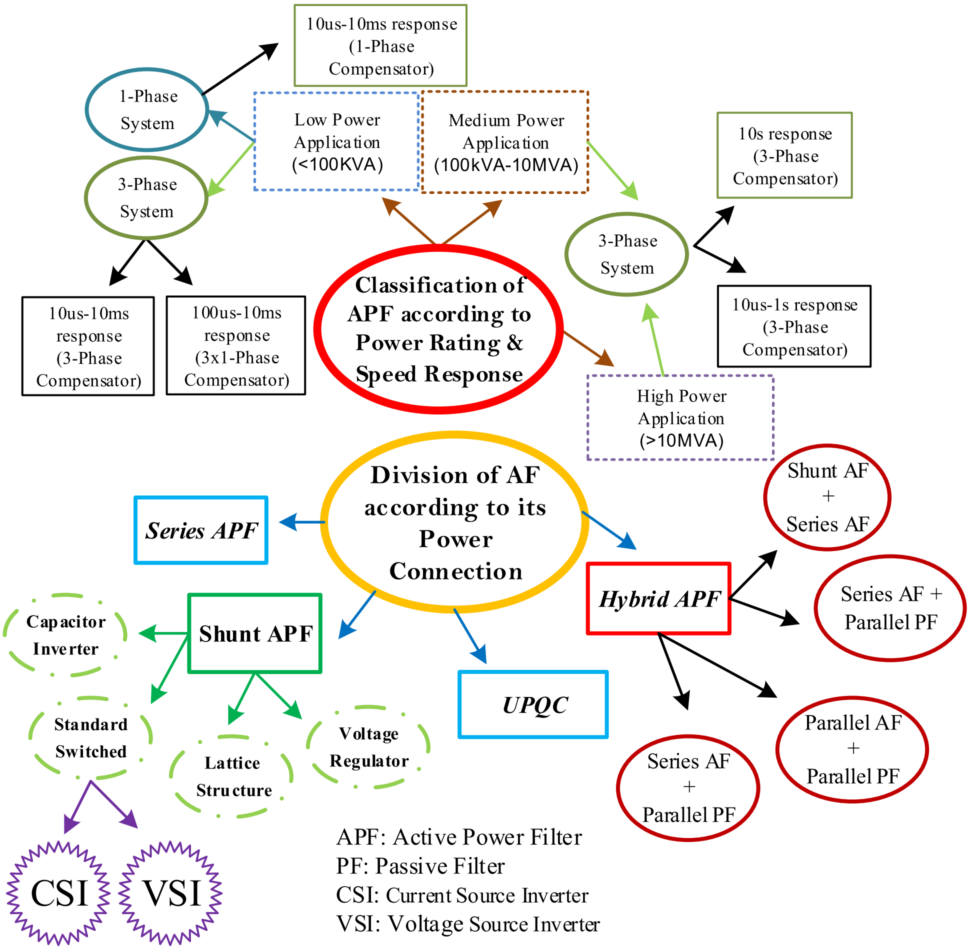

Fig. 2. Classification of APF.

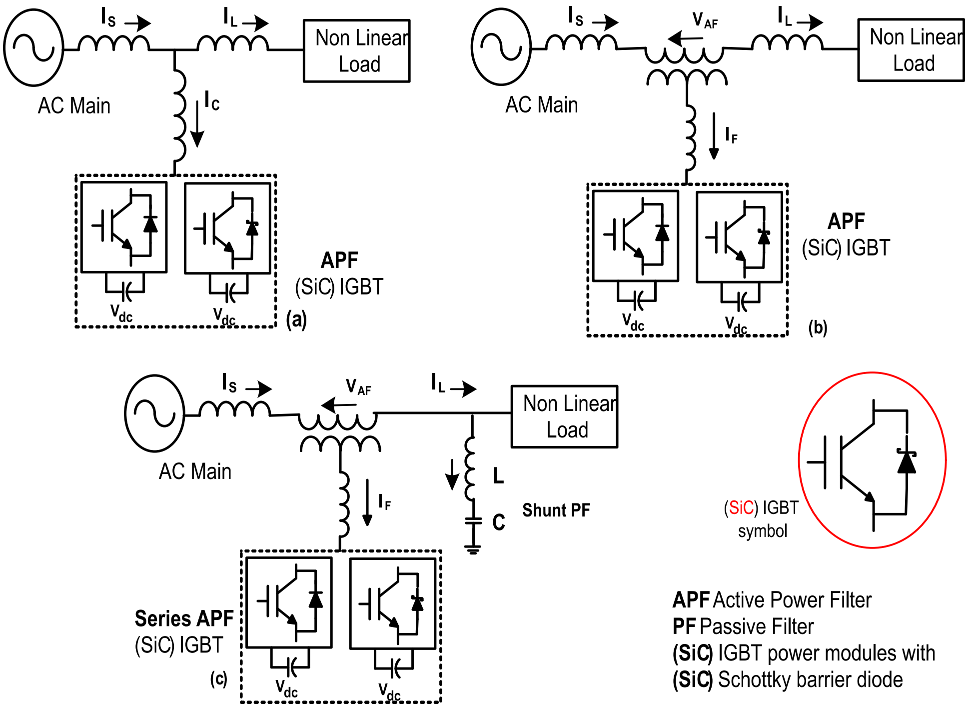

Fig. 3. (a) Shunt APF, (b) series APF, and (c) hybrid APF.

Table 4
Comparison of APF topologies.

Specific Considerations	APF Topology		
	Shunt Active Filter	**Series Active Filter**	**Hybrid APF**
Circuit configuration	Fig. 3(a)	Fig. 3(b)	Fig. 3(c)
Power range			
Small scale	< 350 W (power ratings below 100 kVA)		
Medium scale	< 350 kW (three-phase systems ranging from 100 kVA to 10 MVA)		
Large scale	< 350 kW (systems with ratings above 10 MVA)		
Converter efficiency			
Small	Lowest (up to 98%)		
Medium	High (up to 98%)		
Large	Highest (up to 98%)		
Power circuit	Minor power loop in PWM-VSI	No power loop in PWM-VSI	Minor current loop/No current loop in PWM-VSI
APF operates as	Current source **(CSI)**	Voltage source **(VSI)**	Both **(CSI/VSI)**
harmonics generating Loads	Thyristor/diode rectifier with Inductive load	Diode rectifier with Capacitive load	Thyristor/diode rectifier with Inductive load
Additional function	Reactive power compensation, Current compensation	AC Voltage regulation, Voltage flicker Compensation	Harmonic compensation/ Harmonic damping/ Harmonic isolation
Switching devices	IGBTs, MOSFETs, GTO thyristors	IGBTs, MOSFETs, GTO thyristors	IGBTs, MOSFETs, GTO thyristors
Current harmonics	**	–	***
Reactive power	***	–	**
Load balancing	*	–	–
Neutral current	**	–	*
Voltage harmonics	–	***	**
Voltage regulation	*	***	**
Voltage balancing	–	***	**
Voltage flicker	***	**	–
Voltage sag and dips	*	***	**

High number of "*" is preferred

2.2. Grid-connected APF-WE inverter

In recent times, the energy industry is leaning more toward renewable energy consumption. Wind energy is a more legitimate source of power, less expensive, and available throughout the years [87]. Compared with fossil fuels and solar energy, wind energy has the additional advantage of being cost effective, absence of greenhouse gas emissions, a progressive renewable energy source, accessible and production is flexible so energy demand can be met, and more environment friendly at the power distribution network level [88]. However, power quality is a complicated issue in grid-connected WECS.

The high demand for mounting WTs with the main grid [89] affects the reactive power, voltage fluctuations, flicker because of switching

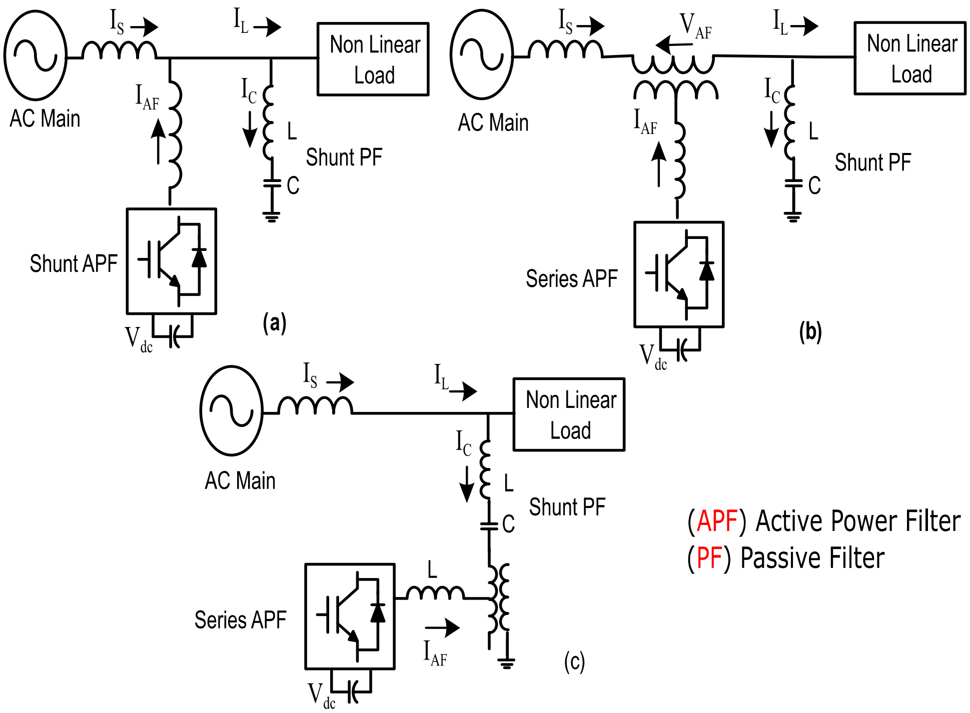

Fig. 4. (a) Shunt APF with shunt PF, (b) series APF with shunt PF, and (c) APF in series with shunt PF.

and during operations, and output voltage and current at the PCC. The variable-speed WT operation depends upon the active and reactive power control and behavior of the nonlinear and unbalanced loads. In this aspect, the nonlinear characteristics of power electronic devices [90] generate high THD value current and output voltage, weakening the WT generator (WTG) performance [91,92], cause more heat and low system efficiency, and decrease the life span of WTG [93]. Therefore, an appropriate harmonic mitigation and reactive power compensation technology is necessary to improve the power quality of wind energy [94] in the grid-connected WECS. A WTG operates at the constant wind speed to control the permanent magnet synchronous generator (PMSG) [95,96] for the APF operation to mitigate the current harmonics A forward modified modulation technique is used to control the APF system based on different reference signal extraction techniques [97].

A more advanced variable frequency-based WT system (WTS) [98] operates in the islanding mode to cancel the harmonics and function of APF. Through the doubly fed induction generator (DFIG) [99] in the fixed speed, WT used the ability of APF under the islanding mode. To reduce the converter cost, a reduced-switch-count topology [100–104] for WECS system is installed. A split-capacitor leg is shared between the back-to-back converters at the area of voltage unbalance. This topology has decoupling issues between the multipole PMSG and the grid. In addition, it requires an extra DC-link capacitor, needs a more complex control, and faces higher semiconductor stress [105].

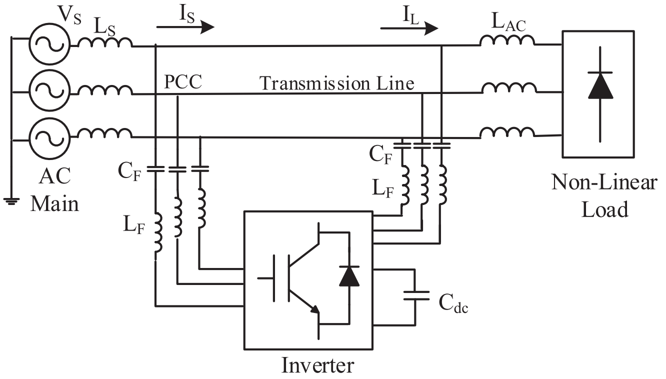

Fig. 6. AC–AC inverter topology.

In grid-connected WECS, reactive power control and compensation is an important requirement and an essential parameter to the power distribution grid. It is essential to maintain the constant voltage profile of the WTG to control the minimum losses in transferring the reactive power exchange to the power grid. The under load tap changer transformer is the main device that controls reactive power compensation in the grid. Furthermore, several WT produce limited voltage and reactive power in the coupled induction generator [106]. As a solution, several devices, such as STATCOM [107], SVCs, on-load tap changer (OLTC) and switching capacitors, PWM inverter, and a combination of capacitor and inductor [108], are installed with the induction generators. Several devices, such as DBR, OLTC, and manual switched capacitor banks, are not capable of overcoming harmonics and voltage flicker. By contrast, the SVC, STATCOM, and DFIG devices improve the static and dynamic stability behavior of the reactive power and fixed

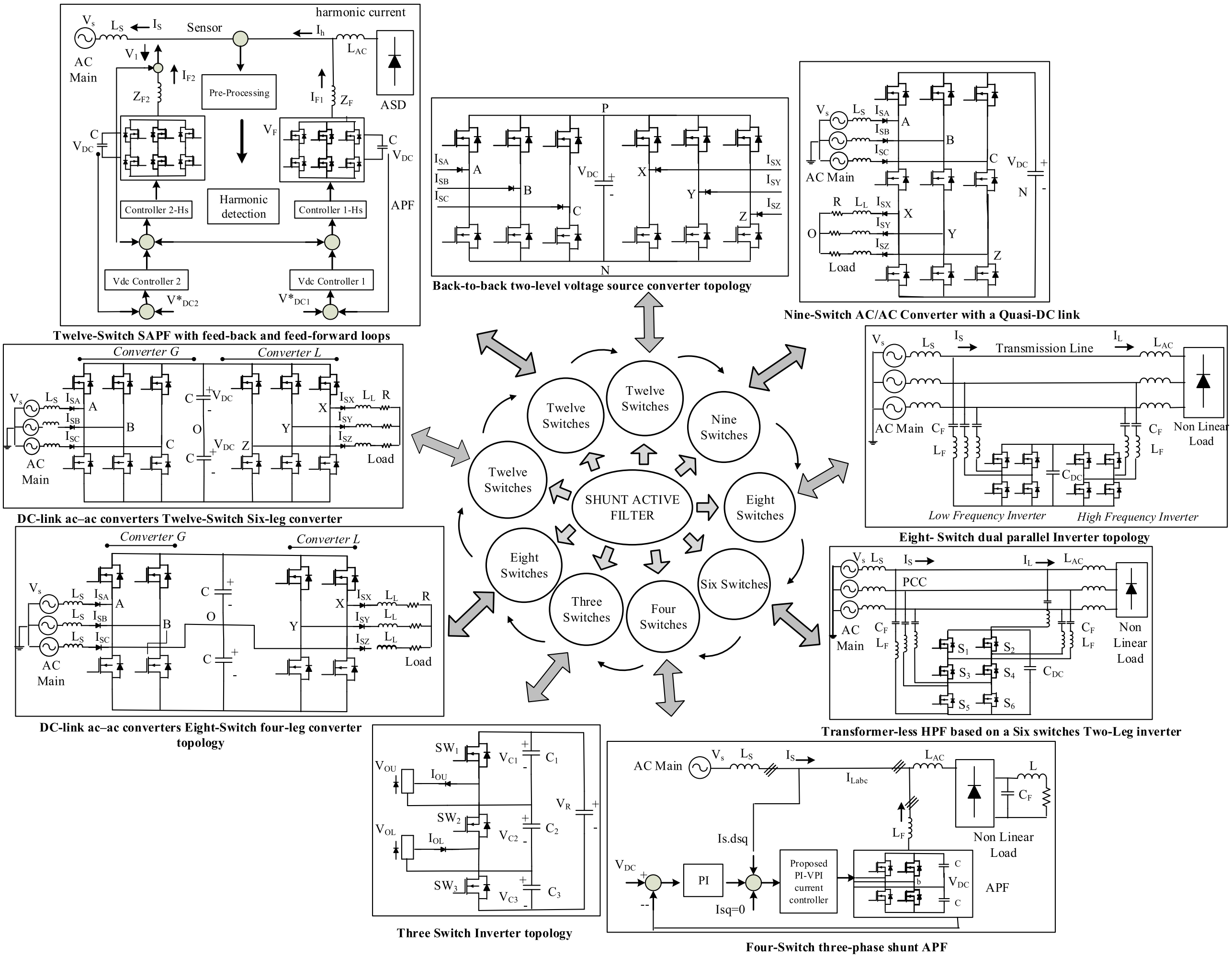

Fig. 5. Overview of reduced switch-count inverter topologies in grid application.

Table 5
Comparison of reduced-switch-count AC–AC inverter topology.

Author	[129]	[130]	[131]	[132]
Topology	One leg	Three leg	Two leg	Two leg
Modulation/control	SPWM/EF-DF	SPWM	PI/VPI current control	SPWM/PI
Capacity (kVA)	2.5	5	1.5	1.8
Switching frequency (kHz)	6	3.2	10	20
Conventional topology	6	12	6	9
Reduced switch count	3	9	4	6
No. of legs	1	3	2	2
No. of filter inductors	1	3	3	6
No. of filter capacitors	+	0	0	6
No. of transmission line inductors	+	3	3	6
Grid voltage (V)	+	208	127	220
No. of DC capacitors	3@2200uF	1@2350uF	2@2000uF	1@4700uF
THD %	60–1%	64.74–1%	24.4–1.89% (RL) 30.2–1.97% (RLC)	36–3% (no load) 43–5.6% (with load)
Estimated efficiency	High	Medium	Medium	Low
DC-link voltage (V_{dc})	200 V	320 V	420 V	120 V
Grid interface	3transistorVSI	6 transistor VSI	4 transistor VSI	3 transistor VSI

+ Not reported, ~ Estimated Value

speed wind generators [109]. However, these devices regulate the voltage balance [110], which helps in increasing the use of the wind power in power grid networks.

Table 3 demonstrates the reactive power compensating devices [111] in grid-connected WECS compared with other parameters [112]. The control parameters related to reactive power compensating devices are as follows: on-load tap changer (OLTC), automatic voltage control (AVC), dynamic voltage restorer (DVR), series dynamic breaking resistor (SBBR), static synchronous compensator (STATCOM), static VAR compensators (SVC) [113], thyristor-controlled series capacitor (TCSC), and unified power flow controller (UPFC).

3. Classification of grid-tied APF

Generally, the APFs are classified into three categories as depicted in Fig. 2, that is, topology- based type, converter type, and a number of phases [114]. The topology-based type category is subclassified into three types: SAPF, series APF, and HAPF. The number of phases (wires) are divided into single-phase (two wires), three-phase (three wires), and three-phase (four wires) systems [115]. The topology-based category is categorized into the shunt, series, and hybrid configuration as shown in Fig. 3. The series APF reduces the negative sequence of voltage harmonic propagation caused by the system resonance [116], which improves the electrical utilities of terminal voltage. In the energy industry, the increasing demand of high load current generates current rating loss and filter size limitation. Table 4 shows the comparison of three APF topologies [117,118].

Three different combinations of HAPF circuit are illustrated in Fig. 4. The series APF with shunt PF offers high impedance for the harmonic isolation in the medium voltage system as depicted in Fig. 4(c). It delivers reactive power, voltage harmonic compensation, and balancing of the three-phase voltages [119–121]. On the other hand, SAPF alongside shunt PF is used to eliminate the fundamental reactive power and high order load current harmonics as shown in Fig. 4(b). In high-power application, both systems provide reactive power compensation with less switching cost [122,123]. In medium- and high-voltage applications, the constant DC-link voltage and grid fundamental voltage are maintained by using series APF together with shunt PF as depicted in Fig. 4(a), which effectively reduces the system volumetric size and cost [21,124].

4. Comparative study on reduced-switch-count APF inverter topologies and their control

This study reviews the three best reduced-switch-count APF configurations in detail, namely, AC–AC inverter, back-to-back inverter, and common-leg inverter topologies. The complete cycle of reduced switch count integrated into grid application, starting from twelve to three switches, is explained in Fig. 5.

4.1. AC–AC inverter topology

In AC–AC inverter topology, the pulse width modulation voltage source inverter [24] is connected in parallel with the DC-link capacitor as illustrated in Fig. 6. Single-phase two-wire, three-phase three-wire, and three-phase four-wire are the respective sections of the AC–AC inverter configuration.

4.1.1. Single-phase (two-wire) APFs

In high-power application, the diode-clamped, flying-capacitor clamped, and switch-clamped inverters use several semiconductor switches. A single-phase six-switch reduced-count VSI without both the clamping diodes and flying capacitors achieves harmonic elimination, reactive power compensation, and inverter losses [125]. In five levels, AC terminal voltage uses eight-switch power converter [126] to eliminate the need for a transformer. To reduce voltage stress, two flying capacitors are used in correspondence with flying-capacitor-clamped and switch-clamped inverters to reduced volumetric size, weight, and cost [127,128]. Four different configurations of AC–AC inverter topology are summarized in Table 5, discussing the number of

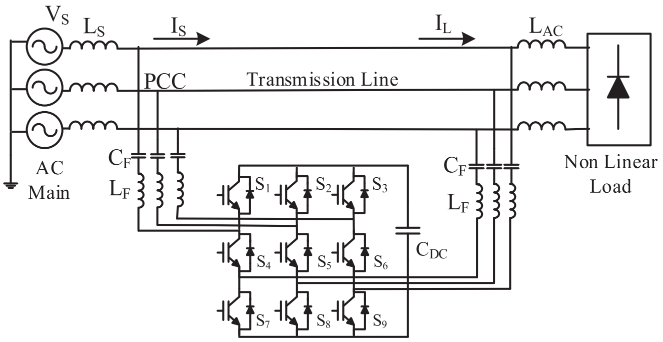

Fig. 7. Nine-switch AC–AC inverter APF circuit.

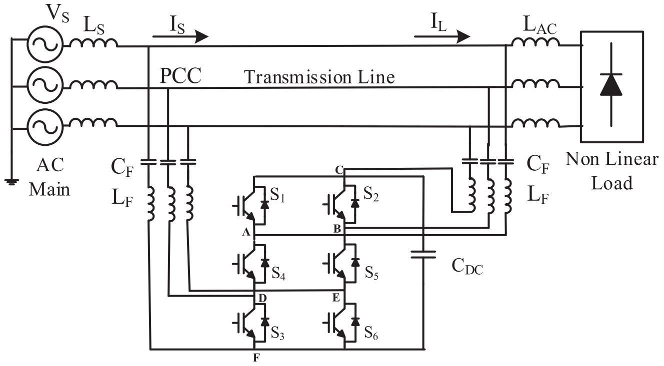

Fig. 8. Six-switch AC–AC inverter APF circuit.

switches, the filter inductors, and different system parameters, such as THD, DC-link voltage, switching frequency, and estimated efficiency.

The bootstrap technique used in three-level current source inverter needs an isolated multiple DC power supply and an electrolytic capacitor. All the circuit switches are connected to common source or common emitter to reduce the gate-drive power supplies into a single power source. the electrolytic capacitor usually has short life span because of its larger size [133]. Regardless, a single-phase three-level converter provides low harmonic content as compared with a two-level converter. The reduction of switches creates three limitations, that is, the need for an isolated DC source, curtailed modularity, and fault-tolerant capabilities [134,135]; reducing the component voltage rating and improving the system power factor effectively eases the system cost, switching loss, and switching state redundancies.

To reduce the system cost, a transformerless single-phase line-interactive uninterruptible power supply (UPS) system is presented in [136–138] to control the DC current and AC current component for the charging and discharging the battery bank. A DC capacitor is connected in series with a three-leg power converter to operate as a buffer in between the switch set, filter capacitor set, filter inductor set, battery set, and decoupling circuits [139,140].

4.1.2. Three-phase (three-wire) APFs

A three-phase APF system consists of four-switch converter and eight-switch converter configurations. It uses a two-arm bridge inverter and a DC-link capacitor to eliminate the harmonics, reactive power problems, and subsequent variations in the DC-link voltage [141–146], aside from removing the current sensors in several applications because of common mode current strategy [146]. The only constraint in high-power applications of the three-phase APF is that it requires high-voltage stress switches because of the large turns on resistance. A soft switching converter technique is used to reduce one-half of DC bus voltage and to increase the total output power [147].

The two-clamping diodes, four MOSFETs, one flying capacitor, and magnetic cores reduce the PWM controller volumetric size and cost compared with the conventional three-level converter. By controlling the output voltage for leading and lagging switching operation [148], at the secondary side, two center-tapped rectifiers reduce the current rating of the rectifier diodes, output filter inductors, and transformer windings, which result in reducing switch voltage stress, zero voltage switching (ZVS), and load current sharing.

Three-phase conventional matrix converter requires eighteen IGBT switches with complex switching scheme. Fifteen switches with reduced-count IGBT switch converter is presented in [149]. Presenting a better reduced switch count, a unidirectional power flow twelve IGBT switches is designed in an ultra-sparse matrix converter [150].

Overcoming the limitation of three-leg nine-switch inverter [130] as depicted in Fig. 7, the improved two-leg six-switch inverter is presented in [132]. Fig. 8 demonstrates an HAPF topology connected to a three-phase load without using the matching transformer consisting of a two-leg six-switch reduced inverter connected in series with two passive LC filters. Tuned at different harmonic frequencies, it provides better compensation than both the conventional HAPF topology and the three-phase VSI topology.

Another pair of reduced-switch-count dual-leg six-switches and the single-leg three-switch leg structure topologies are connected to a two individual single-phase loads [129,151]. Moreover, the single-leg inverter operates as a two half-bridge inverters with minimum achievable three switches split capacitors technique as depicted in Fig. 5 (three-switch inverter topology). Both systems operate independently as a two full-bridge and half-bridge inverters connected with single-phase and three-phase critical loads.

4.1.3. Three-phase (four-wire) APFs

To control and compare common mode space voltage, a four-switch scalar PWM vector control method is used by contrast with the standard six-switch three-phase inverter [152]. In the three-phase four-wire system, a neutral current circulates beside the reactive power, load current harmonics, and unbalance current. The unbalanced current is caused by the negative and zero-sequence current components. To compensate, a three-phase four-wire (3P4W) SAPF is designed for the multiple power-quality problems in three different configurations, that is, split capacitor (2C), four-leg (4-leg), and three-H (3HB) bridge structure for nonlinear loads [152].

In general, all the three-phase current-controlled VSI-PWM converters are twelve or eight switches [153,154], but in the proposed design, it uses six switches with two split DC-link capacitors shared by both the rectifier and inverter [155–158]. The DC-link capacitor leg acts as neutral point connection for reducing the number of switches. To minimize the undesired negative effect and zero-sequence current in the four-wire APF system, a zigzag transformer is used. An interleaved inverter is proposed to cancel the triggered effect of power transmission lines, nonlinear loads, asymmetrically phased load, and power harmonic current quality [154–156]. The interleaved inverter generates higher switching losses than the conventional two-level inverter in terms of DC-link capacitor losses [157]. Five-level and three-level inverter circuit consists of a reduced number of switches in the induction motor drive as parallel to the conventional cascading two-level and three-level neutral-point clamped (NPC) inverters. To overcome the problems of bearing current, shaft voltage, early motor failure, and common-mode voltage (CMV) variation, a DC voltage control and CMV elimination method [159] is adopted.

An alternative concept discussed is the combination of the diode clamp-type topology with a flying capacitor-type topology; a four-switch converter replaces the twelve-switch converter with lesser number of diodes [160]. The operating limits in the semi-bridged rectifier system require a tradeoff between current distortion and switching ripple [161]. By doubling the switching frequency, this tradeoff and dead time distortion is improved. ZVS converter uses soft switching technique to reduce the number of power switches and

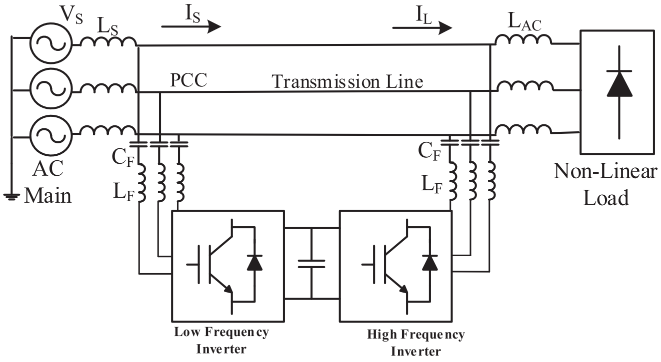

Fig. 9. Parallel inverter topology.

Table 6
Comparison of reduced-switch-count back-to-back inverter topology.

Author	[172]	[173]	[174]
Topology	H-bridge	H-bridge	Full bridge
Modulation/control	SPWM/PI/Feedforward and feedback	SPWM/PI	SPWM/PI/Feedforward and feedback
Capacity	3 kW	3.3 kVA	15 kVA
Switching frequency (kHz)	550 Hz and 20 kHz	550 Hz and 20 kHz	12.6 kHz
Conventional topology	12	12	12
Reduced switch count	8	8	12
No. of legs	4	4	6
No. of filter inductors	5	6	6
No. of filter capacitors	5	6	6
No. of transmission line inductors	9	6	6
Grid voltage (V)	110	110	300
No. of DC capacitors	1@4700uF	2@3300uF	2 @ 4.4mF
THD (%)	4.70% 23.50%	0.03%	1.26% 1.11%
Estimated efficiency	Medium	High	Low
DC-link voltage (V_{dc})	26	1500	400
Grid interface	4 transistor VSI	4 transistor VSI	6 transistor VSI

+ Not reported, ~ Estimated Value

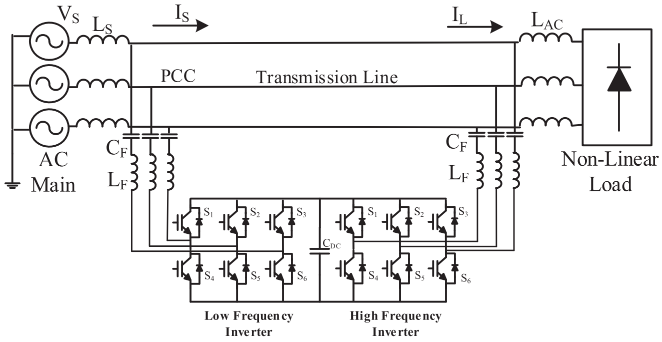

Fig. 10. Twelve switch parallel inverter APF circuit.

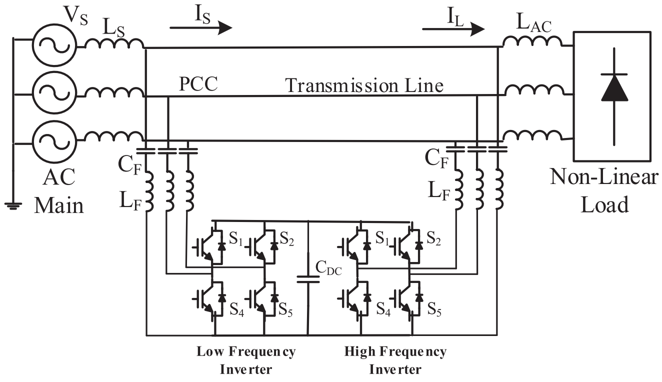

Fig. 11. Eight-switch parallel inverter APF circuit.

output current ripple. To balance the two input capacitor voltage, a three DC–DC circuit is designed to reduce the three-level diode clamped with two flying capacitors [162].

4.2. *Back-to-back inverter topology*

Fig. 9 illustrates the three-phase three-wire back-to-back inverter topology. Both inverters are connected back-to-back with the common DC-link capacitor. The main advantage of this configuration is that it improves the APF compensation capability.

4.2.1. *Single-phase (two-wire) APFs*

The dual-leg six switches operate similarly to the two full-bridge inverters for two single-phase load. Without a matching transformer, the single converter and maximum power flow strain the system performance. As a solution, a reduced-switch-count universal APF is designed to convert the single-phase into a three-phase system [163]. A transient time delay occurs in a half-bridge UPS system because of power failure [164,165]. To improve the system response, a reduced switch count of two and three-leg UPS system is presented in [166–169]. In offline UPS system, a simple winding is added in series with the common transformer to eliminate the switches [170]. An improved switch-reduced three-leg inverter structure is presented in [171] to control one leg as a boost converter to boost the DC-voltage, whereas the other two legs operate as a full bridge inverter. It operates as an active filter in normal mode and battery charger in the backup operating mode. Three different back-to-back inverter configurations are evaluated based on reduced switch count and detailed in Table 6.

To strengthen this observation, another reduced half-bridge UPS configuration with eight switches including four-switch converter and four-switch inverter was used. Also, it eliminates the isolation transformer because of the common input and output neutral point [175]. As presented in [176–178], reduced number of switch count eliminates the need for circuit breakers and static switches, as compared with the conventional line-interactive or online UPS schemes.

4.2.2. *Three-phase (three-wire) APFs*

A dual HAPF inverter topology consists of two power converters in a back-to-back configuration, sharing a common DC-link capacitor as depicted in Fig. 10. The feedforward and feedback control is adopted for switching operation. In high-dynamic load systems, larger capaci-

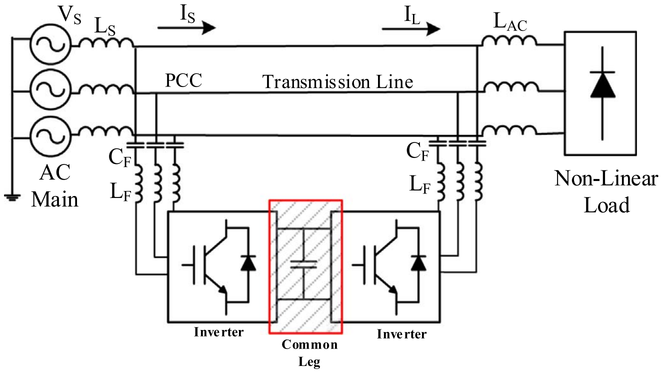

Fig. 12. Common-leg inverter topology.

Table 7
Comparison of reduced-switch-count common-leg inverter topology.

Author	[193]	[194]	[195]
Topology	Four leg, Three leg, Five leg	Five leg	Six leg
Modulation/control	SPWM	SPWM	SPWM/PI
Capacity	~1.5 kVA	~1.5 kVA	5 kVA
Switching frequency (kHz)	5	10	12
Conventional topology	+	12	12
Reduced switch count	8, 6, 10	10	12
No. of legs	4, 3, 5	5	6
No. of filter inductors	+	3	12
No. of transmission line inductors	3	+	6
Grid voltage (V)	60	100	400
No. of DC capacitors	2@1000uF	2@2200uF	1@2.2mF
THD (%)	0.8% (8 switches) 0.6% (6 switches)	1.54% (1st experiment) 0.8% (2nd experiment)	27–2%
Power factor [PF]	+	0.997	+
Estimated efficiency	High	Medium 0.84 (1st experiment) 0.9 (2nd experiment)	Low
DC-link voltage (V_{dc})	100	200	250
Grid interface	2 transistor VSI, 2 transistor VSI, 4 transistor VSI	4 transistor VSI	12 transistor VSI

+ Not reported, ~ Estimated Value

tors and DC bus voltage are needed to maintain the larger stability margin to keep less voltage stress across each capacitor. A split capacitor (B4) topology is adopted [179] with low cost and losses via the limitation of voltage balancing across the DC-link capacitor. As a solution, the third phase is connected to the neutral midpoint of split capacitor legs, which reduces the twelve-switch power converters to eight-switch configuration.

Presenting a better reduced-switch-count topology, the third phase is connected to the negative pole of the DC link [172,180] intense some limitation of split capacitor topology as depicted in Fig. 11. Despite complex control and hardware design limitation, it improves the system reliability, lowers cost, and preserves low-voltage stress across the DC capacitor.

Upon further investigation, the LC PF is tuned at 550 Hz to eliminate the lower-order harmonics and maintains the DC-link voltage constant. The higher-order LC PF is tuned at 750 kHz to eliminate high-level harmonics. A single current sensor is used to connect the current source feedforward control and voltage source feedback control for active filtering [174]. Both controls provide a steady-state and dynamic response for harmonic mitigation.

A dual four-switch reduced count in each bridge inverter is proposed as compare with the conventional twelve-switch dual-bridge inverter [181,182]. To improve harmonic compensation and keep the grid in stable operation, a load sharing and frequency sharing is done with and without the redundancy in both the filters. The common mode voltage and circulating current at the DC-link capacitor generates numerous problems, that is, premature motor bearing failures, voltage fluctuations at DC side, limited power rating components, and EMI. To stop the zero sequence, which is the current circulating between inverters, separate DC capacitors or transformers are installed [180]. In line-interactive UPS topology [183], series-parallel power converters are connected in bidirectional three-leg and two-leg configurations [179]. By adding three more switches to the unidirectional three-phase seven-switch resonant inverter, a bi-directional power flow is achieved [184] to operate at zero voltage and high-frequency AC link.

4.2.3. Three-phase (four-wire) APFs

Another reduced UPQC system is presented in [185], which is achieved by connecting the neutral terminal to the negative end of the DC capacitor. The proposed neutral-clamped UPQC system reduces the number of components [186], DC-link voltage, average switching frequency, and THD in source current. For the independent control of each leg, a capacitor voltage balancing is needed for shunt and series inverters, increasing the size and cost of the system. A three-phase *voltage source converter* distributed static synchronous compensators and T-connected transformer (Scott-*T transformer)* are installed to reduce the system size. To match the DC-link voltage of APF system, supplementary capacitors are installed in series with a common capacitor and inductor.

4.3. Common-leg inverter topology

Fig. 12 illustrates the three-phase three-wire common-leg inverter topology in back-to-back configuration. The circuit is designed by sharing the common DC-link capacitor via single- or double-leg sharing between the APF rectifier and inverter. Usually, the common leg switches operate during the rectifier and inverter operations. Single-phase (two-wire) and three-phase (three-wire) configurations are discussed below.

4.3.1. Single-phase (two-wire) APFs

Two DC-link five-leg and six-leg configurations are designed in parallel to a single-phase two-wire APF system via single-leg inverter sharing. It includes a coupling inductor and DC-link capacitors [187,188] to reduce the system components rating. A universal APF consists of shared leg between the half bridge and full bridge inverters for voltage and current harmonic compensation. A parallel series injection transformer is used as a source for power factor control [189].

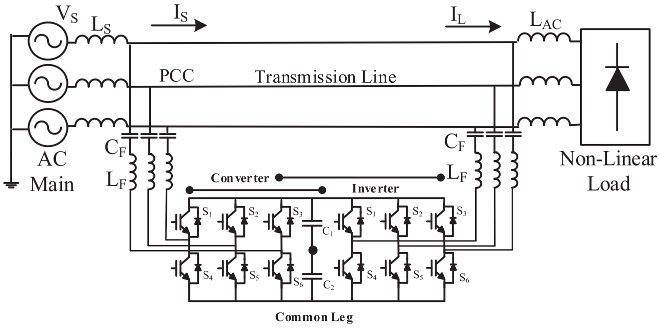

Fig. 13. Twelve-switch common-leg inverter APF circuit.

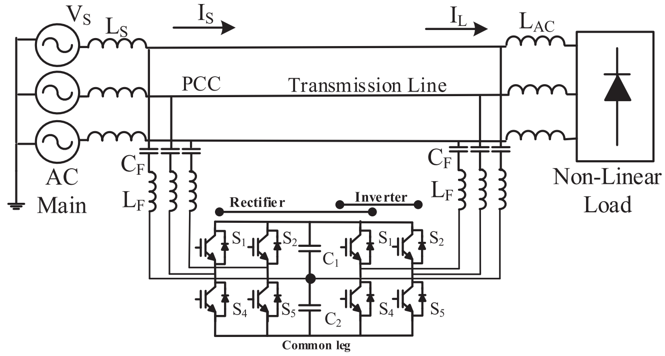

Fig. 14. Eight-switch common-leg inverter APF circuit.

Table 7 summarizes the comparison of three common-leg H-bridge topologies. The six-switch three-arm bridge voltage regulator reduces switching devices with low-cost AC capacitors. It controls unity power factor, sinusoidal input current, output voltage regulation, and bidirectional power flow [190]. A single-phase three-leg converter shares a leg between the source and load. It reduces the six-switch three-leg converter into a four-switch two-leg converter structure [191,192].

A single-phase online UPS system provides high efficiency, high power, and quick response to voltage disturbances. A common leg is shared between the rectifier and inverter to provide the bidirectional current flow. The first rectifier leg is used to charge the battery bank, the third inverter leg is used to control the output voltage, and the middle leg is used for controlling the line frequency [196]. The common leg reduces the number of switches at low-power losses, low-cost structure, and reactive power control.

4.3.2. Three-phase (three-wire) APFs

A total of nine switches are installed on a three-leg converter circuit, but the middle leg is shared between the rectifier and the inverter circuits [193]. Input and output power is delivered from the middle switches. Quasi DC link through a two constant frequency and variable frequency mode provides unity power factor, sinusoidal input, and output waveform. A Two-level twelve-switch converter as depicted in Fig. 13 contributes to cutting down manufacturing cost as compared with the matrix eighteen-switch converters. Nine-switch converters produce the same AC voltage level with an oversized DC-link capacitor, which overstresses the semiconductor switches. IGBT devices require higher switching ratings and generate higher losses compared with back-to-back twelve-switch converter, along with limitations such as limited amplitude sharing and phase shift in the output terminal [194].

A single auxiliary switch replaces the two independent auxiliary switches to improve the power density of the DC–DC converter. A soft switching with zero voltage transition and zero current transition technique is adopted alongside high switching losses and electromagnetic interferences [197,198].

In another single-phase to three-phase AC motor drive system, multiple legs connected between the grid and load are shared. They are reduced to eight switches in a four-leg configuration. Both the converters are based on reduced switch as compared with the ten-switch configuration by sharing the single leg [195,199–201] as depicted in Fig. 14.

Different four-leg, five-leg, and six-leg converters with controlled gate-drive circuit, diodes, and power supplies are reduced by sharing the common leg. It increases the common-leg current and reduces the DC voltage [202–204], which improves system losses, fault error tolerance, installation size, switch, and capacitor current rating [205,206].

Two voltage-source APFs are connected to the power line through common-mode coils and DC-link capacitor to reduce the size of passive components [207–209]. The common mode coils replace the isolation transformer, which provides smaller volumetric-size inductors.

A phase-leg averaging technique is used to reduce the size and cost of the system without using any passive components in both the individual converters. To eliminate the passive LC filter, the control is designed with space-vector modulation through a high-bandwidth control loop to suppress the circulating current [210].

5. Analysis and discussion

5.1. Reduced-switch-count inverters

Based on the above analysis, a comparison among the various transformerless and reduced–switch-count grid-connected inverter topologies has been summarized in Table 8.

It is noticed that to produce AC-voltage amplitudes in back-to-back topology, a much larger DC-link capacitor and DC voltage is needed. This high voltage generates switching losses because of overstress across the semiconductor switches. To overcome this problem, z-source network and discontinuous modulation scheme are implemented [211]. By contrast, the B8 converter configuration practices eight switches with shared split DC link [200]. By sharing a common single DC bus between two individual converters, the B8 converter creates a large DC voltage variation in the value DC link and lower AC voltage in the output. However, no fundamental current flows through DC link if both the system is functioning and synchronized at the same frequency. On the other hand, to overcome the B8 converter limitation, a five-leg converter is introduced by sharing the fifth-phase leg between the two converter interface [212]. Roughly, no large DC variation is observed in fundamental voltage, but it has the limitation of the common frequency imposition in between the two AC-interfaced systems, including applications like series-shunt power conditioners and adjustable powered speed drives.

Recently, the evolution of SAPF in grid-connected and renewable energy conversion system became important because of power-quality-related problems. Over the last years, several conventional and advanced topologies and control methods have been documented for capacities, harmonics mitigation, reactive power compensation, and auxiliary functionalities. Table 9 summarizes the conclusions and parameters based on the recently developed APF topologies described in Section 4. Each topology is evaluated and compared with each other to select low-cost, efficient, and suitable configurations. The following conclusions are drawn from this review:

1. The traditional back-to-back power converter topology is limited by an oversized DC-link capacitor, limited amplitude sharing, and uncontrolled phase shift between the two converters at output terminals sets.
2. The back-to-back topology offers less complicated and independent control for the two individual decoupled converters. It is limited by low modulation ratio which causes computational problems [213] in spite of topological aspect. Different frequencies and limited phase-shift constraint put a limit on maximum modulation ratio and requires the addition of the triple offset to avoid the crossover.
3. Reducing the switches improves the total efficiency, and lessens dissipated conduction and switching losses, but this is subjective to the quantity of the switches. In high-power rated system, all switching components are under high-voltage and current stress, which eventually affect the inverter performance.
4. The AC–AC topology shows limited phase shift and strict amplitude sharing in between the two terminal sets, such as dual motor drives [167], rectifier–inverter systems, and UPS [214].
5. By sharing the carrier at two converters, output terminals set for same output voltages and the DC-link voltage and semiconductor stress doubled. This doubling effect is removed in reduced-switch-count topologies.

Performance comparison among the three different reduce-switch-

Table 8
Evaluation of reduced switch count APF topologies.

Ref.	Modulation/ control	Capacity (kVA/kW)	Switching frequency (kHz)	Actual topology	Reduced switches	No. of diodes	No. of filter inductors	No. of filter capacitors	No. of transmission line inductors	Grid voltage (V)	Trans- former	No. of DC capacitors (μF)	THD (%)	DC-link voltage (V_{dc})
Single-Phase System														
[125]	Hysteresis	≤7.5	10	8	6	0	1	0	1	311	0	2@2000	6.5	375
[129]	SPWM/EF-DF	2.5	6	6	3	0	1	-	-	-	0	3@2200	2	200
[151]	Hysteresis	-	7	12	8	0	1	0	-	60	1	1@1100	3.77	115
[164]	SPWM/PI	≤1	20	4	2	0	1	1	-	110	0	3@3000	7.3	316
[171]	SPWM/PID	3	16	8	6	0	3	1	-	100	0	1@-	3.20	170
[175]	SPWM/PI	≤1	10	6	5	1	1	0	-	120	0	2@-	-	350
[176]	PWM/PI	1	10	8	6	0	1	0	1	120	0	2@-	3.54	700
[190]	SPWM/PI	1	5	8	6	0	1	1	-	100	0	1@-	0.58	200
[196]	SPWM	3 VA	15	8	6	0	1	0	-	220	0	1@1880	3.5	192
[170,171]	SPWM	250 VA	1	8	5	1	1	0	-	220	1	-	-	39
[191]	Hysteresis	1	10	8	6	0	1	0	-	100	0	2@2200 ,	0.85	200
[188]	PWM/PI	1	10	8	8	0	1	1	1	200	1	2@2200	1.15	380
[220]	PWM/PI	-	-	12	9	0	3	0	-	380	1	2@1000	3.16	
Three-Phase System														
[14]	SPWM/Adaptive DC-link	-	7.5	8	6	0	3	3	3	55	0	2@190	3.00	40
[130]	SPWM	5	3.2	12	9	0	3	0	3	208	0	1@2350	2	320
[131]	PI/VPI current	1.5	10	6	4	0	3	0	3	127	0	2@2000	1.89 1.97	420
[132]	SPWM/PI	1.8	20	9	6	0	6	6	6	220	0	1@4700	3 5.6	120
[221]	SPWM/PI	4	20	6	4	0	3	3	3	220	0	1@2200	4.96.	400
[141]	SPWM/PI	7	20	6	4	0	3	3	3	380	0	1@4700	4	370
[143]	Hysteresis	5	7.0–9.1	9	6	0	3	0	-	110	0	2@2200	3.6.	400
[146]	SVPWM/PI	2	20	12	8	4	3	0	3	110	0	2@2200	3.10	400
[149]	SVPWM	6.8	10	18, 15	15, 9	18, 18	-	3, 3	-	400	0	-	-	-
[154]	SV/PWM	7.5	7.2	16	12	6	4	4	-	400	0	1@4.4mF	6.08	700
[152]	SVPWM/PQ	20	7	8	6	0	4	0	4	35	0	2@1200	4.91	125
[153]	Hysteresis	15	6.85	8	6	0	4	3	-	-	0	2@4.4mF	6.88	700
[156]	SVPWM	50	6.4	6	4	0	3	0	-	380	0	2@5000	17.8	1400
[161]	SVM/SPWM/PI	1	10	24	12	36	3	0	-	200	0	8@47, 100, 220	3.40	-
[172]	SPWM/PI/FF & FB	3	550 Hz/20	12	8	0	5	5	9	110	0	1@4700	4.70 23.50	26
[173]	SPWM/PI	3.3	550 Hz/20	12	8	0	6	6	6	110	0	2@3300	0.03	1500
[174]	SPWM/PI/FF & FB	15	12.6	12	12	0	6	6	6	300	0	2@4.4mF	1.26 1.11	400
[181]	PWM	1KW	6	9	6	0	6	0	3	200	0	3@2200, 1100, 2200	1.50	208
[189]	DEAD-BEAT	3	15.6	-	6	0	6	3	3	110	1	2	2.66	720
[193]	PWM	~1.5	5	-	8, 6, 10	0	-	-	3	60	0	2@1000	0.8 0.6	100
[194]	PWM	~1.5	10	12	10	0	3	0	-	100	0	2@2200	1.54 0.8	200
[195]	SPWM/PI	5	12	12	12	0	12	0	6	400	0	1@2.2mF	2	250
[157]	SPWM/Adaptive DC-link	10	5	8	6	0	4	3	3	200	0	2@3.3mF	4.5	75
[222]	SRF-LS-PWM	1	1	18	12	24	3	0	-	60	0	4	5	200
[163]	SPWM/PI	3	10	12	10	0	3	0	-	110	1	2@2200	1.65	140
[185]	PI/ HYSTERESIS	5	3.10–6.8	12	12	0	6	6	6	230	1	1@2200	2.80	225, 125
[203]	SPWM/PI	2	5.2	10	8	0	3	3	3	100	0	2@2200	-	260

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Table 8 (*continued*)

Ref.	Modulation/ control	Capacity (kVA/kW)	Switching frequency (kHz)	Actual topology	Reduced switches	No. of diodes	No. of filter inductors	No. of filter capacitors	No. of transmission line inductors	Grid voltage (V)	Trans-former	No. of DC capacitors (µF)	THD (%)	DC-link voltage (V_{dc})
[144]	SVPWM/PI	2	20	12	8	4	3	0	3	110	0	2@2200	4.20	400
[137]	SVPWM/PI	10	7.5	6	6	0	3	3	3	400	0	1@25	5.90	300
[186]	SPWM/PI	1	-	16	14	0	6	6	-	100	1	1@5000	2.30	220

count topologies is summarized in Tables 5–7. They are evaluated on based on amount of reduced switches, efficiency, component ratings, and THD. It was observed in studies [130] and [131] that they have moderate efficiency because of a high number of inverter switches. However, three switches had the highest estimated efficiency (94–96%) [129], although it had high-rating components. As noticed, the reduction of switches and inverter legs highly affects the voltage rating and DC-link capacitor size. In fact, distributed between the inverter legs, the conventional inverter topology demonstrates a low DC-link voltage as compared with reduced–switch-count topologies [130]. To compensate for the effect of reduced switches, the DC level is aided by the combination of series capacitors, thus increasing the number of active and passive components [131], which contributes to higher system cost [132].

Another back-to-back topology has been proposed in Ref. [174], which tested low-rating components to generate high output power (15 kVA) and mitigate harmonics. In practice, Ref. [173] demonstrated the highest estimated efficiency based on the design of eight switches as compared with other configurations. A greater number of switching components [172] produces more switching and conduction losses, thereby lowering the inverter efficiency [174]. In the evaluation stages, Ref. [172] demonstrated a medium level of efficiency with extra single DC capacitors as compared with Ref. [174]. By contrast, the APF mitigate the grid-connected harmonics [173] to maximum achievable level of 0.03% (grid current) as compare to results reported by other studies [172,174].

A recent advancement for the common-leg inverter topology is dynamically researched and presented in existed previous report [193]; maximum efficiency is achieved with the grid current THD values of 0.8% and 0.6%. Compared with another report [194], this topology has 6 switches and 28 total estimated components with medium efficiency. The authors modeled the APF system for low efficiency [195], this work aimed to reduce the number of inverter switching components (15 components), with a THD value of 2%. In grid-connected PV and WECs with AFP, the target of reducing the number of switches is directly related to the output value of the DC-link capacitor. The main topology consists of a single capacitor, which needs high-power IGBTs and a DC-voltage rating to increase the voltage stress, cost, and complexity of the inverter.

5.2. Grid-connected PV inverter

In some studies, the SAPF circuit topologies are similar to the grid interactive inverter to mitigate the harmonics and offer better power quality in the power distribution systems. To fix the high inverter cost and great number of components, several PV grid interactive system are combined to improve the reliability and efficiency of the system. In this manner, utility grids are integrated with the transformerless multilevel and multifunctional inverters based on the APF in the PV and WECS.

To reduce the cost, volumetric size, and weight of the inverter stage in grid-connected systems, the transformerless configuration is considered an excellent solution in the PV inverters. However, the elimination of a transformer causes the absence of galvanic isolation [215], thereby causing an induced leakage current, unstable common mode voltage (e.g., efficiency degradation and safety problems), and safety hazards. The H5 transformerless inverters topology [216] is designed for high efficiency [217] to suppress the leakage current and reduce the leakage current. The main difficulty in this topology is that the leakage current still remains high during the freewheeling mode because of the existence of junction capacitance between the switches [218]. By contrast, to overcome the voltage fluctuating issues, two techniques are implemented. First, during the free-wheeling periods, the PV panels are disconnected from the grid. Second, the neutral wire is used to connect with one pole of the PV panels. The most interesting feature of cascaded H-bridge topology is the high efficiency and to

Table 9
Conclusions and remarks for reduced switch count APF configurations.

Ref	Switches	Control	Action performed	Problems	Solution	Comments
[132]	Six switches	Synchronous DQ	The single leg is removed to connect the single phase to the middle point in the system.	The imbalanced DC-link voltage is caused by sharing the same DC-link voltage in six switches of a two-legged structure.	The phase terminal is connected to the negative or positive pole of the dc link, thereby inducing the circulation of the dc current and the injection of a grid dc voltage in the system. Capacitors are used between the DC-link poles and PCC. The LC-filter capacitor reduces the dc current and DC-link voltage.	Problems, such as the voltage balance across the DC-link capacitor and the DC-link voltage imbalance, are encountered.
[129]	Three switches	Pulse width modulation (PWM); reference shifted	By removing the circuit legs, two dual-legged and single-legged switches are reduced to count the topologies of six switches and three switches in the leg structure.	By reducing the number of switches, the consumable switching states are limited as compared with the traditional fully decoupled converter topology, thereby avoiding the dc-bus short circuit and floating of loads.	Two modes of operation are achieved in the upper and lower loads of the current path by switching the state frequency independent of the output voltage. The inverter operates in all ON and OFF states. Both outputs are zero when the switches of the same row are OFF. When the upper and bottom layer of switches are ON, the others are working in the operating states. The corresponding output is in zero state. When both outputs are in the active state, the opposite switches of the two legs are OFF.	Problems are avoided by coordinating the two modulating references per phase across the upper and lower terminals. Hard switching operation occurs.
[131]	Four switches	Proportional–integral (PI)/vector proportional–integral (VPI)	The accuracy of the system is affected by extracting the harmonic components in the load current. The reference filter current depends on the current controller and the harmonic current detector. A slow response time and steady-state response was observed when adaptive filters in the control were used. These filters affect the accuracy of APF.	By eliminating the need for a harmonic detector, the need for a current sensor is minimized. The control of the performance of harmonic tracking is unaffected by the proposed control.	By applying indirect current control schemes, the harmonic detector is eliminated without requiring the load current. The proposed PI/VPI controllers indicate the direct supply of current, which is regulated according to the change in the fundamental reference of harmonics. The controller uses the minimum current sensors and conventional four-switch three-phase inverter to mitigate the harmonic current and reactive power, as well as simplify the hardware structure. The overall cost is reduced and the accuracy of the APF system is improved.	The overvoltage spikes are higher. Lower costs and smaller sizes are achieved because of the lower rating.
[172]	Eight switches	Feed forward and feedback	By connecting both inverters in the back-to-back topology with parallel DC-links, such that both operate in parallel at different switching frequencies. The number of switches is reduced by eliminating the complete leg from both VSI inverters.	The high voltage across the DC-link capacitor creates a voltage balance problem, thereby affecting the stability of the overall system.	The system aims to connect the phase in the negative or positive pole of the DC-link.	For the present problems, this paper does not consider the distortion of the source voltage and reference dc-bus voltage. Given the lower limit on a DC-link capacitor, a theoretical value of the voltage ripple is restricted to 2% half cycle at the fundamental. or affecting frequency.
[174]	Twelve switches	Master–slave	To reduce the system cost, both inverters are connected in a feedback and feed forward loop configuration by sharing a single load current sensor and a single DC-link capacitor.	Complicated control produces a zero-sequence current circulation between inverters.	The proposed control operates at both filters as frequency- sharing or load-sharing, with or without redundancy. The feedback configuration provides the steady-state operation of harmonic mitigation.	The need for an isolation transformer to stop the circulation of the zero sequence current between inverters is eliminated. Several of advantages over the single unit inverter APF include the reduction of line current ripple and grid high frequency

(continued on next page)

Table 9 *(continued)*

Ref	Switches	Control	Action performed	Problems	Solution	Comments
					The feed forward filter configuration improves the dynamic response of the system. Both controls operate as a current source and a voltage source.	losses, as well as the loading of harmonic compensation and EMI. This treatment reduces the size and cost of the switching ripple filter by combining a single DC-link.
[130]	Nine switches	Sinusoidal PWM (SPWM)	By sharing the rectifier and inverter, the middle switches were used in each leg of the nine switch converters. The power and voltage are delivered via these middle switches and the dc-capacitor.	The input/output voltage control is performed by three switches per phase on each leg. By sharing the middle switches between the rectifier and inverter, the inverter leg voltage cannot exceed the rectifier leg voltage.	Proper inverters and the DC equalizer push the rectifier-modulating wave. At any time, the rectifier modulating wave should not be lower than the inverter modulating wave. The modulating waves are prevented from intersecting with each other.	The diode rectifier B2B 2L-VSC is replaced with the PWM voltage source rectifier with the DC-link capacitor because the DC-link capacitor has a limited lifespan.
[194]	Ten switches	PWM	The proposed circuit shares a common leg to reduce the number of power switches	The cost and number of power conversing devices, like power switches, are reduced.	By reducing the size of the gate driver circuit, the five-leg circuit with an increased power rating provides better performance as compared with the six-leg circuit when the load frequency is equal to the grid frequency power.	The grid and load converter voltages do not depend on the individual capacitor voltage. This value fluctuates between the rectifier and the inverter. The AC does not flow through the DC-link capacitors.
[195]	Twelve switches	Synchronous DQ reference frame	By interconnecting the two voltage-source APF inverters, the system components are reduced by the common-mode coils and a DC-link capacitor.	The single dc-capacitor creates a conduction path between the two inverters, thereby producing a circulating cross-current, which is equal to the switching frequency.	Common mode coils replace the isolation transformer to provide minimum bandwidth, a simple and flexible circuit, faster harmonic tracking response, smaller line inductance, and harmonic current compensation during any module failure. Interleaving reduces the inductor size, line-current ripple, and switching stress in the DC-link capacitor; higher switching and controller bandwidth is achieved in high-power applications.	The core saturation in the isolation transformer limits the switching frequency. The degree of each inverter current is higher because of the lower boost inductor and total current ripple. Each inverters is tuned at the half-rated power because of sharing the common load, thereby increasing the controller bandwidth, with high switching frequencies.
[193]	Eight, six, ten switches	PWM	By sharing a common leg, both the inverters are connected as single-phase to two-phase systems and single-phase to three-phase systems	The harmonic voltage pattern changes because of the distributing factor (THD) by varying the freewheeling period The range of the distributing factor is difficult to select for the given mutually dependent grid and load	The flow of fundamental AC is stopped by the DC-link capacitor. The circuit provides a smaller THD. The stable input/output voltage converters are controlled.	Its complex PWM requires more complex and complicated control to effectively produce zero sequence current problems.

boost the AC side output voltage levels, with a disadvantage of excessive amount of switches [219].

An alternative is the high efficient and reliable inverter concept (HERIC) [216] and H5 inverters, especially in the half-bridge topologies. The neutral point is connected to the midpoint of the input voltage, but requires synchronization between gate signals. Therefore, a special circuit based on six switches and two diodes in the transformerless PV inverter suppress the leakage current and stable common mode voltage. To improve the leakage current, enhanced multi-level inverter topologies are installed rather than the conventional topologies.

6. Future work

As previously mentioned, the inverter is a major component for the efficient harvesting of renewable energy in the PV and WT energy conversion system. To increase the output efficiency and minimum power loss, the system inverter must minimize the semiconductor devices and number of switching components. This approach produces the next-generation high-powered and high-temperature semiconductor devices, such as the packaging of silicon carbide (*SiC*) IGBT power modules with Schottky barrier diode (SBD) modules and SiC MOSFET. The inverter is a topic of concern in the solar cells/panels because of its relatively low efficiency as compared with wind energy sources. The SiC devices exhibit higher efficiency and increases the power-to-weight ratio of the system, thereby resulting in minimum inverter cost. On the other hand, transformerless inverters are the most appropriate technique pertaining to grid-connected PV APF systems. The inverter ensures DC/AC power conversions with minimal interference by the grid, with other advantages such as high efficiency gains, Volt/VAr control (power factor correction), voltage stability, frequency regulation, empowered energy storage, and low system cost.

Recently, multilevel inverters have become more attractive in the field of renewable energy grid-connected systems. In high-voltage rated systems, the multilevel converters have an advantage over the conventional two-level topology. Low-voltage components are used in each module but with higher amounts. Thus, the output harmonic distortion and filter size are reduced. Continuous monitoring of the unbalanced DC-link capacitors and complex control schemes are required as a constraint. This step requires a higher amount of feedback sensors, thereby increasing the cost and complexity of the circuit structure. The dual-terminal inverters, shared legs between inverters and rectifiers, and the substitution the split capacitors configurations are topics of interest for further research.

7. Conclusions

This paper provides the state-of-the art and strong perspectives on the transformerless, passive components of APF and grid-connected renewable energy systems. This review provides a broad perspective to researchers, manufacturers, and engineers who deal with harmonics and power quality issues. To enhance the power quality of the DER and DPGS, innovative and novel developments have been reported in the field on grid-connected inverters. The main research trends related to the reduced switch count inverters with APF topologies include the back-to-back inverter, AC-to-AC inverters, and common-leg inverter configurations. Therefore, the PFs, APF, HAPF, hybrid filters, UPQC, and STATCOM are considered as power quality improvement techniques. APFs are mature technologies that act as a powerful bridge between distributed grid systems and harmonics pollution. To date, a large number of well-developed and large-capacity advanced APF technologies are available in the market for consumers. The demand for APFs has been reviewed to reduce the power semiconductor components, auxiliary circuits, and coupling transformers in terms of the cost, volumetric size, weight, THD, power loss, and efficiency. Additionally, the present grid-connected APF PV inverters and wind energy conversion inverters are investigated, analyzed in detail, compared, and discussed. To sustain the power quality at an acceptable level in the long run, the utilities will encourage the installation of APF technology alongside the nonlinear loads. The new APF principles described in this article are SVG and STATCOM. The APF is an effective solution for power quality problems, such as harmonic mitigation, voltage regulation, load balance, power factor correction, and neutral current compensation, in grid-integrated distribution systems. Therefore, the dual-terminal inverters, shared legs between inverters and rectifiers, and substitution of the split capacitor configurations are potential techniques for advanced SAPF systems.

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