Hybrid HTS-FCL Configuration With Adaptive Voltage Compensation Capability

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***Abstract*—This paper introduces a new hybrid high-temperature superconducting (HTS) fault current limiter (FCL) for improving the transient response system recovery with minimum utilization of HTS material. The hybrid HTS-FCL comprises a reduced size of HTS material connected in series with multistep braking resistors. The presented hybrid HTS-FCL utilizes the fast quench phenomena of HTS materials to ensure fast current limiting action and the multistep braking resistors to provide an adaptive voltage compensation during voltage dips. This combination of HTS and braking resistors allows the HTS material to recover faster by lowering its operating time, mitigates the issue of slow response in conventional braking resistors, and keeps the system fault level below the maximum limit even during offline recovery of its HTS component. A dynamic model representing the hybrid HTS-FCL is developed in PSCAD/EMTDC using a current-dependent model for the HTS combined with dynamic braking resistors associated with a phase voltage control scheme and an HTS bypass scheme for each phase individually. The proposed configuration is tested in a single-machine-to-infinite-bus test system in response to symmetrical and asymmetrical fault conditions. A comprehensive simulation analysis demonstrated the effective performance of the hybrid HTS-FCL with capability of fast fault current limitation and voltage boosting.**

***Index Terms*—Angular stability, dynamic braking resistor high-temperature superconductor, hybrid fault current limiter (FCL), voltage recovery.**

I. Introduction

MODERN POWER systems struggle to meet the rising energy demands without risks on the system's security and reliability. One of the main challenges is the escalating short-circuit levels due to the increased penetration of distributed generation, grid interconnections, expansions in power plants, and more importantly, circuit breakers' down rating [1]. Thus, fault current limiting is one of the most important issues for power system operators. Usually, fault levels are operationally maintained by a number of operational methods such as bus splitting, generation-constrained dispatching, and network splitting [1], [2]. Eventually, these approaches lower the network's stiffness and introduce further limitations on daily operations. Currently, fault current limiters (FCLs) are employed within power networks to mitigate fault levels. Of all FCLs, series reactors are the most used FCL, although they impose permanent impedance in the network, which degrades the voltage profile and system stability and causes power losses during normal operation.

To avoid such impact, FCLs have to be invisible in nominal operation without impacting their fault limiting capabilities during fault conditions. Hence, high-temperature superconducting (HTS) FCLs are well recognized as the leading FCL technology in the future. With very fast quenching, resistive nature, and high limiting capabilities, HTS-FCL can control fault levels and enhance system stability [3], [4].

To obtain a reliable HTS-FCL, several things have to be considered:

1) fast limiting action (first peak limitation, to avoid stresses on system equipment);
2) high limiting capabilities, to accommodate for future escalation in fault current levels;
3) fast recovery with capability to withstand successive fault incidents and the operations of transmission line auto reclosers.

The first two points are already achievable by most HTS-FCLs, as given in [5] and [6]. However, fast recovery is considered as the most challenging issue for manufacturers as the quenched superconductor has to be disconnected from the system and cooled down to return to its superconducting state. Thus, the power system will be at risk during offline recovery of HTS-FCL. To further illustrate this point, fault levels have to be maintained within the limit of the interrupting capabilities of the network's circuit breakers at all operating times [2]. If the fault level exceeds these capacities, circuit breakers attempt to fault clearance will fail, and most probably, serious damages will occur. In many researches [7]–[9], HTS-FCLs were proved to provide superior fault limiting capability and enhanced stability performance for generator's integration. However, these studies do not provide post fault analysis to cover the impact of superconductor's recovery on system performance. Practically, recovery is of great importance in situations where the fault occurs at a different line and the HTS-FCL respond to that fault. Therefore, the HTS-FCL will be switched off until it recovers to a superconducting state (usually by a bypassing switch [10]), leaving the system unprotected from high fault levels until the HTS-FCL returns back to service. This is considered as a potential drawback of installing HTS-FCLs as such operation cannot be acceptable by power utilities. A simple solution to this is to install FCLs under N-1 contingency criteria, but it will be a very costly approach. Several papers have addressed the problem of HTS recovery. In [5], a 2G HTS FCL configuration is tested under a certain reclosing scheme, and its recovery performance was thoroughly investigated. It is shown that recovery under load time significantly varies depending on load current and

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baseline voltage. To avoid long recovery duration, a hybrid SFCL scheme with very fast recovery was presented and tested in [11]–[13]. It relies on the HTS element to transfer the fault current after the first peak to a shunt reactor by triggering a fast switch. Although it could achieve a very rapid recovery, it is not capable of mitigating the first peak fault current, which is the highest. Hence, it will impose huge stresses on system equipment.

Since superconductors' recovery is an issue in quench-based FCLs, superconductors were utilized in a different way in a none-quench-based FCL like, i.e., magnetic (saturated core) FCLs, where a superconducting coil is used only in superconducting mode to reduce the size and losses within a dc coil that controls the iron core inductance. However, these types of FCLs are bulky and produce pulsating inductive impedance, which raises the stability and protection concerns associated with them [14].

In [15], SFCL was combined with a parallel-braking resistor to enhance system stability and provide better damping. The proposed configuration relies on SFCL to mitigate power imbalance during the full duration of fault and on the parallel-braking resistor to operate afterward until system oscillations die out. An improvement on system stability is achieved, but no advantage can be gained in terms of superconducting recovery time.

Series-braking resistors are very useful for stability enhancement, and unlike parallel-braking resistors, they can be used to act during fault to provide energy balance and enhance the machine's critical clearing time [16]–[18]. In this type, a resistor is put in parallel with a conventional mechanical switch that can be controlled by a fault-triggering scheme, but it has very slow response time. Further research shows that the series-braking resistor's performance can be significantly enhanced by the use of solid-state switches such as insulated-gate bipolar transistors [18].

In comparison with reactors or MFCLs, the existence of a series-resistive element during fault (either in the form of an SFCL or a series-braking resistor) can dissipate the accumulated power in the generator and retain balance in the system [19]. This paper presents a new hybrid HTS-FCL configuration where the HTS element is combined with multiple steps of series-braking resistors. As the drawback of dynamic braking resistors is that they require a relevantly long switching time, which is not sufficient to tackle the fast limitation of the first peak of fault current, the fast limiting action will be achieved by the HTS element, and thereafter, the fault current will be limited by the stages of a braking resistor until the HTS wire recovers. Eventually, this will keep the system fault level within acceptable limits at all operating conditions. Furthermore, it will not require a very high impedance ratio between the HTS module and the series resistor as in standard SFCLs [6]. Subsequently, it reduces the size of HTS-FCL and significantly improves the recovery time. The new configuration is introduced and modeled in PSCAD/EMTDC, where comprehensive analyses are carried out in a single-machine-to-infinite-bus test system to evaluate the significance of such configuration in reducing the fault current and improving recovery time, voltage compensation, and system stability.

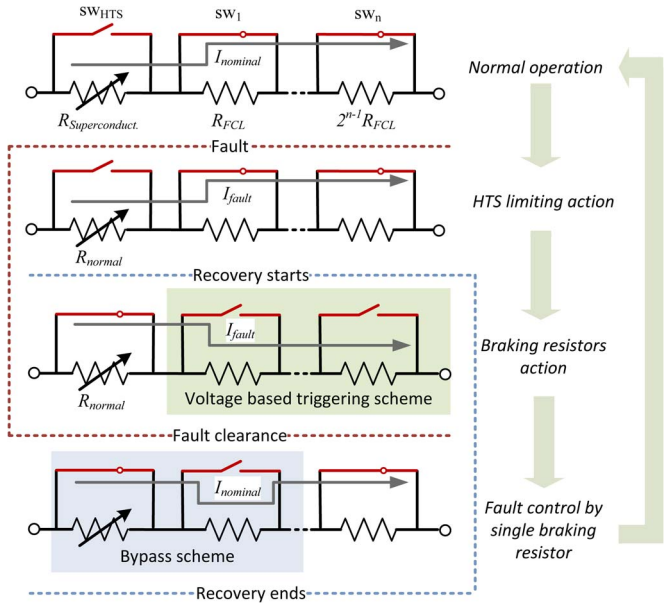

Fig. 1. Hybrid HTS-FCL operation.

II. Hybrid HTS-FCL Configuration

The proposed configuration relies on improving the energy balance according to [19]

$$\frac{2H}{\omega_o}\frac{d^2\delta}{dt^2} = P_m - P_e \tag{1}$$

where:

H inertia constant of the machine;
ω_o normal speed of the machine;
δ rotor angle of the machine;
P_m mechanical power input of the machine;
P_e electrical power delivered from the machine.

Equation (1) represents the deviation in rotor angle of the synchronous machine connected to an infinite bus (grid). At normal operating conditions, mechanical and electrical power is equal, and the machine rotates at normal synchronous speed. When power imbalance occurs, the machine will either accelerate or decelerate. During faults, load instantly drops, whereas the mechanical power remains constant as the prefault power (due to the slow response of mechanical systems) resulted in accelerating the rotor [20]. To maintain the rotor speed, electrical power has to be raised as fast as possible to evacuate the mechanical energy and retain the energy balance in the system.

One way of achieving this is by dissipating this active power using a resistor, and this what makes resistive HTS-FCLs act as stabilizers. Hence, the fast transition of superconductors from a superconducting state to a normal state during faults makes HTS-FCL perfect for these kinds of applications. Nevertheless, superconductors suffer from safety limitations with respect to fault duration [5], and to avoid that, current will be transferred from the HTS wire to the braking resistors within few cycles, such that power dissipation will exist until fault is cleared.

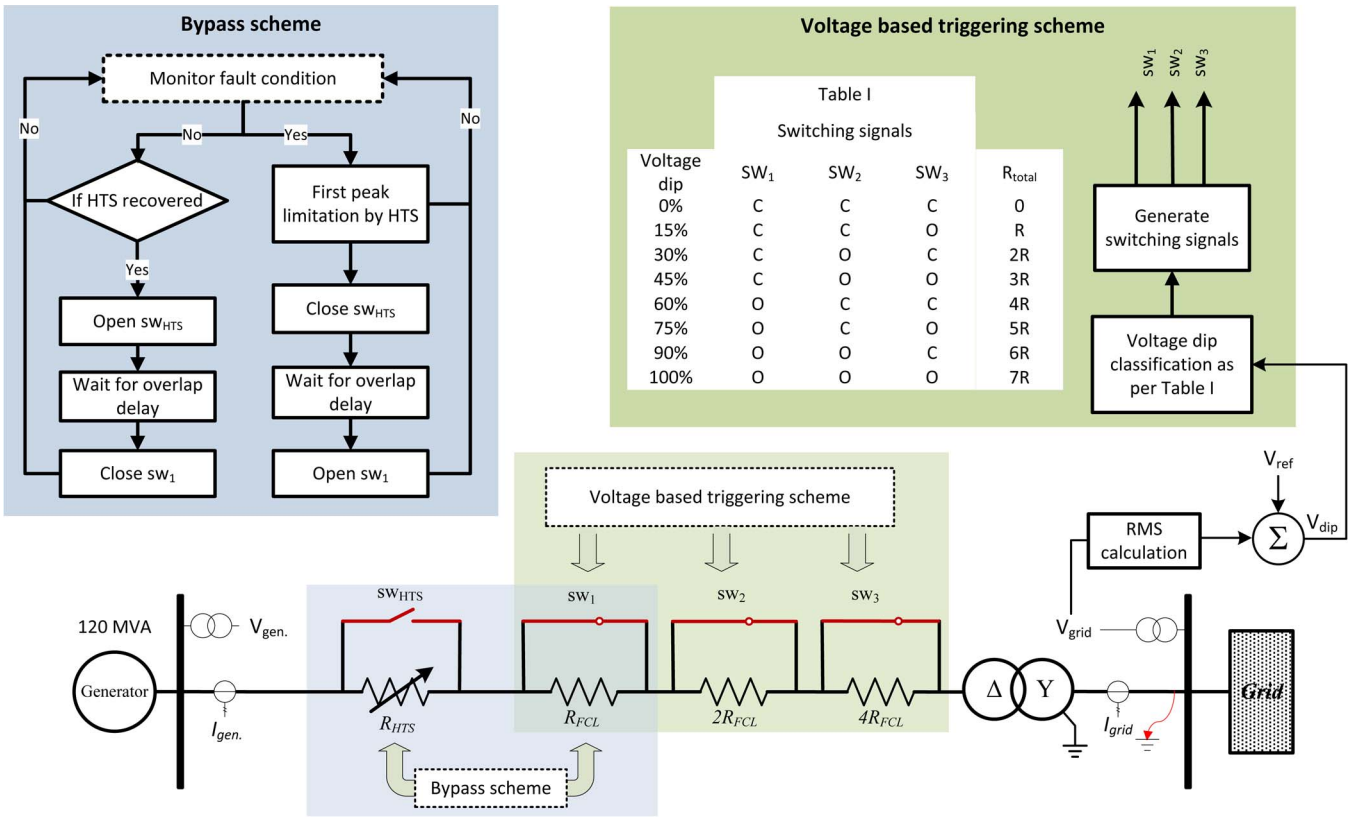

Fig. 2. Hybrid HTS-FCL configuration (per phase).

A. *Hybrid HTS-FCL Operation*

Fig. 1 shows the operation of the hybrid HTS-FCL. The HTS module is connected in series with n number of braking resistors parallel with triggered fast switches.

In normal operation, the power flows through the HTS module, and all braking resistors are bypassed. Once a fault occurs, the HTS module will quench within 1–3 ms, and the voltage-based triggering scheme will trigger the switches of the braking resistors, and the fault detection scheme will bypass the superconductor. Once the fault is transferred to the braking resistor, the HTS module will start cooling down. When the fault is cleared, the braking resistor (with minimum resistance) will remain in service until the superconducting state is reached to maintain the system's fault level under control during the HTS recovery process. However, it can cause slight overvoltage if not properly rated. Hence, the limiting resistor during post fault operation must have an impedance equal to that of the HTS normal resistance, and this impedance has to be carefully chosen to limit the fault current and to avoid the unacceptable overvoltage after fault clearance, as discussed in Section IV. For more adaptive response, a higher number of braking resistors that are controlled by a phase voltage control scheme is recommended to allow smoother voltage recovery. Although, a single braking resistor maybe sufficient according to the system characteristics as will be investigated in this paper.

The proposed three-step hybrid HTS-FCL relies on two switching schemes, as shown in Fig. 2. The first switching scheme is the HTS bypass scheme, which ensure fast disconnection of HTS after quench occurrence and reinsertion of the HTS module after full recovery. The second switching scheme is the voltage-based control scheme, which controls the voltage compensation from the braking resistors until fault clearance is deployed according to the dynamic compensation strategy shown in Table I in Fig. 2. The dynamic braking resistor relies on the logic design of n number of switches, whereas the number of compensation stages is equal to $(n^2 - 1)$. Hence, a higher number of switching elements will provide a wider range of compensation levels. For achieving a higher variety of compensation steps, the resistances' values are adjusted in a ratio of $1:2:4$, as given in Table I in Fig. 2.

III. Power System Modeling

A. *Modeling of HTS-FCL*

The proposed HTS-FCL can be modeled using a combination of three switched resistors controlled by a voltage control mechanism and a variable resistor that represents the HTS quench by the following equation [21], [22]:

$$R_{\mathrm{HTS}}(i) = R_{\max}\frac{\left(\frac{i}{I_Q}\right)^k}{1+\left(\frac{i}{I_Q}\right)^k} + R_{\mathrm{SC}} \tag{2}$$

where R_{HTS} is the variable resistance that ranges from superconducting-state resistance R_{SC} to normal-state resistance $\mathrm{R}_{\max}$, I_Q is the critical quenching current (2 pu), and k is the exponent that controls the steepness of the transition (it is

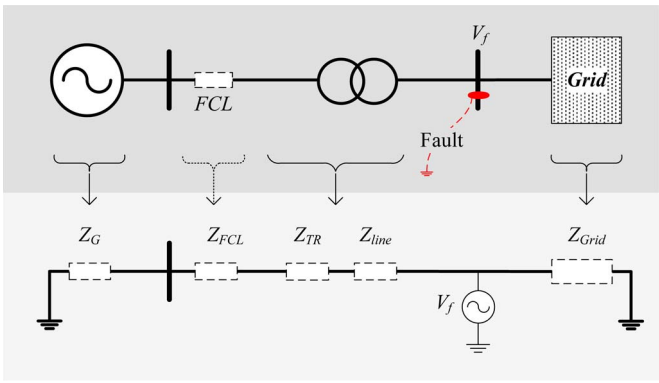

Fig. 3. "Equivalent source" at fault location for a single-machine-to-infinite-bus system with FCL.

set to 24). The model in (2) employs a fast transition (1–2 ms) as soon as i exceeds I_Q.

The required impedance of the FCL should be determined according to the worst-case fault current level. In most cases, symmetrical three-phase faults cause the most significant fault current to flow in the system. Three-phase initial fault current can be determined using the circuit depicted in Fig. 3 that represents the voltage source equivalent of the test system shown in Fig. 2 in accordance with the IEC 60909 standard [23], [24], i.e.,

$$I''_{kk} = \frac{CV_f}{Z_{kk}} \tag{3}$$

$$Z_{kk} = (X''_d + Z_{\mathrm{TR}} + Z_{\mathrm{line}})//Z_{\mathrm{Grid}}. \tag{4}$$

The three-phase initial fault current (I''_{kk}) is calculated using the prefault nominal system voltage (V_f) multiplied by voltage factor (C), and the equivalent system impedance seen at the faulted bus is (Z_{kk}). In this case, system impedance is composed of the machine's subtransient reactance (X''_d), line impedance (Z_{line}), and transformer impedance (Z_{TR}). In the presence of an FCL, the total impedance increases to reduce the fault current.

The FCL impedance can be calculated using the desired reduction in fault current as given in (4), i.e.,

$$\Delta I''_{kk} = I''_{kk} - \frac{CV_f}{Z^{\mathrm{FCL}}_{kk}} \tag{5}$$

$$Z^{FCL}_{kk} = (X''_d + Z_{\mathrm{TR}} + R_{\mathrm{FCL}} + Z_{\mathrm{line}})//Z_{\mathrm{Grid}}. \tag{6}$$

R_{FCL} rating can be calculated using (5) and (6). Therefore, $R_{\max}$ will be set such that R_{HTS} in (2) reaches R_{FCL} in sufficient time to reduce the first peak current. Thus, For HTS with very fast quenching time (1–3 ms), $R_{\max}$ can be directly set to R_{FCL}. The multistep resistors will be designed using 1 : 2 : 4 ratio to achieve resistances of R_{FCL}, 2 R_{FCL}, and 4 R_{FCL}, which will range from 0 Ω (during bypass operation) up to a maximum resistance of 7 R_{FCL} at the worst voltage dip.

B. Test System Modeling

The test system consists of a salient-pole synchronous machine connected to an infinite bus through a Δ/Y transformer.

TABLE I
SYNCHRONOUS MACHINE PARAMETERS

State variable	Definition	
ψ_{1q}	Flux linkage of q-axis damper winding	
ψ_{1d}	Flux linkage of d-axis damper winding	
E'_q	Transient voltage in q-axis	
δ	Rotor angle	
ω	Rotor speed	
Parameter	**Description**	**Value**
T''_{do}	Sub-transient time constant of d-axis	0.039 s
T''_{qo}	Sub-transient time constant of q-axis	0.071 s
T'_{do}	Transient time constant of d-axis	6.55 s
X_d	d-axis reactance	*1.014 pu*
X'_d	d-axis transient reactance	0.314 pu
X''_d	d-axis sub-transient reactance	0.28 pu
X_q	q-axis reactance	0.77 pu
X''_q	q-axis sub-transient reactance	0.375 pu
X_l	Stator leakage reactance	0.163 pu
ω_s	Synchronous rotor speed	$2\pi 50$ rad/s
k_D	Damping coefficient	0
H	Inertia constant	3.117 s
Signals	**Definition**	
T_m, T_e	Mechanical and electrical torques	
I_d, I_q	d-axis and q-axis currents	
E_{fd}	Field voltage obtained from the exciter	

TABLE II
EXCITER PARAMETERS

Parameter	Description	Value
T_1	Smoothing time constant	0.02 s
T_A	Lead time constant	1.5 s
T_B	Lag time constant	1.0 s
T_E	Exciter time constant	0.02 s
K	Exciter gain	100 pu
V_{ref}	Reference voltage	1.0 pu
Signal	**Definition**	
E_m	Measured voltage	

The hybrid HTS-FCL will be connected in series with the generator at the medium-voltage side.

A $dq0$-transformation is performed to model the synchronous machine. The direct axis defines the magnetic axis of the rotor, and the q-axis leads the d-axis by 90° with respect to the direction of rotation following [25]. Accordingly, the detailed fifth-order model was developed considering three windings, of which damper winding and field winding exist on the d-axis, and one damper winding exists for the q-axis. As common practice, network and stator transients are neglected, leading to the following model (parameters are given in Tables I and II):

$$T'_{do}\frac{dE'_q}{dt} = E'_q - (X_d - X'_d) \times \left[I_d - \frac{X'_d - X''_d}{(X'_d - X_l)^2} \times \left(\psi_{1d} + (X'_d - X_l)I_d - E'_q\right)\right] + E_{fd} \tag{7}$$

$$T''_{do}\frac{d\psi_{1d}}{dt} = -\psi_{1d} + E'_q - (X'_d - X_l)I_q \tag{8}$$

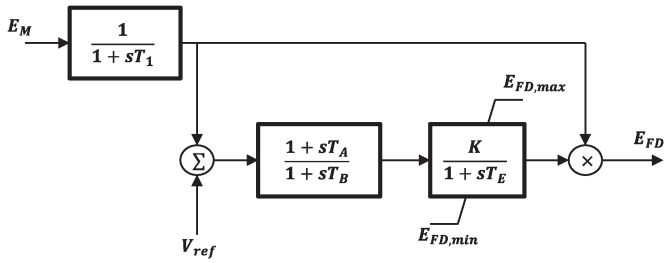

Fig. 4. Solid-state exciter model.

$$T''_{qo}\frac{d\psi_{1q}}{dt} = -\psi_{1q} - (X_q - X''_q)I_q \tag{9}$$

$$\frac{d\delta}{dt} = \omega - \omega_s \tag{10}$$

$$\frac{2H}{\omega_s}\frac{d\omega}{dt} = T_m - T_e - k_D\omega. \tag{11}$$

Equations (7)–(9) represent the dynamics in the d- and q-axes, whereas (10) and (11) represent the swing equation.

The excitation system plays a vital role during transients. Thus, the synchronous generator was equipped with a solid-state excitation system to regulate the field voltage [26]. The solid-state (or bus-fed) exciter's model is presented in Fig. 4.

IV. System Evaluation and Simulation Results

The proposed configuration was tested on a single-machine-to-infinite-bus test system shown in Fig. 2. The test system is comprised of a 120-MVA synchronous machine connected to the electric grid through a 13.8/230-kV Δ/Y transformer with the hybrid FCL connected at the medium-voltage side. The hybrid HTS-FCL has three stages of braking resistors with $R_{\rm FCL}$ set to 0.2 Ω following 1 : 2 : 4 ratio and total delay time of 20 ms, which accounts for measurement and switching delays. A 2-ms overlap time is allowed between HTS and braking resistors to avoid any unprotected period during system operations.

A. Symmetrical Fault Condition

Single- and multistep hybrid FCLs are tested and compared in response to three phase-to-ground faults for a duration of six cycles. In Fig. 5, the fault resulted in 100% voltage dip in the stator voltage and 25-kA fault current measured at the medium-voltage side. Hybrid multistep, single-step, and standalone multistep (without HTS) schemes are alternatively employed to mitigate the fault current and provide voltage compensation in response to grid fault. Both hybrid FCLs (single-step and multiple-step) are capable of reducing the fault current to below 17 kA due to the fast quench of the HTS component incorporated with the FCL, as shown in Fig. 5(a). This fast action is clearly visible in the voltage measurement where the compensation is immediately started at 0.4-pu voltage. However, the standalone multistep braking resistor shows a slower response (20 ms) until the switching operation is started. Thus, the reduction in the first peak current was negligible, as shown in Fig. 6(a).

The highest voltage compensation was achieved by a hybrid multistep FCL since it can build up its resistance by the HTS

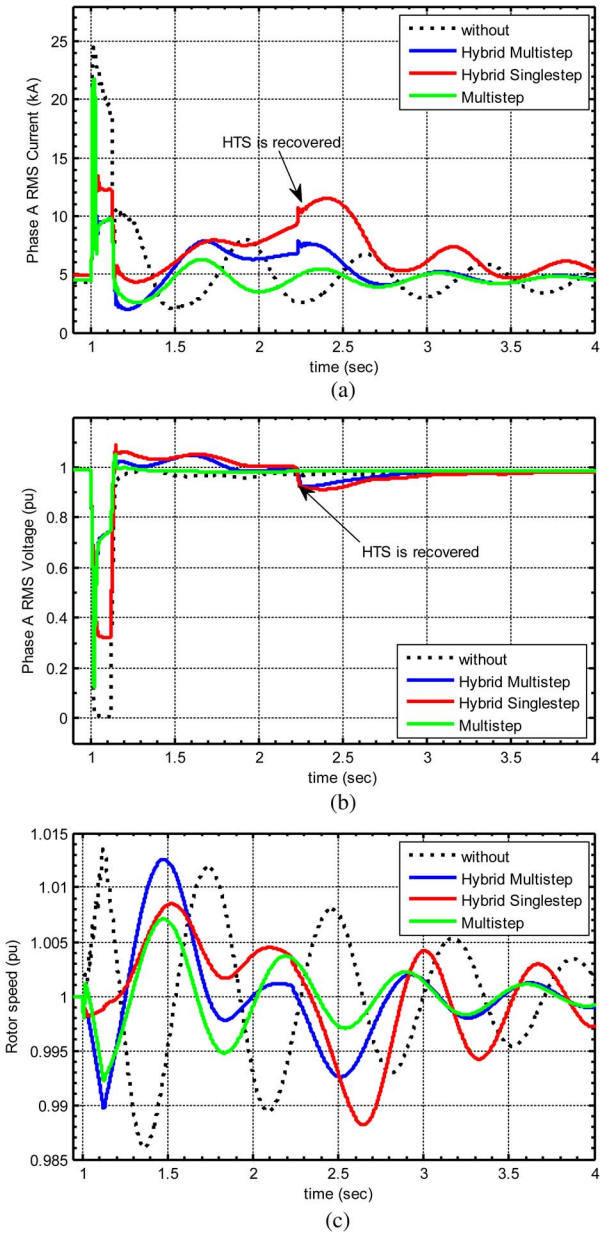

Fig. 5. Phase-A signals.

quench almost immediately after the fault occurrence. Once the HTS is deactivated (bypassed), both hybrid and standalone multistep provide typical voltage compensation, as shown in Fig. 6(b). With regard to transient stability, the rotor speed of the synchronous machine is accelerated without compensation to above 1% until the fault was cleared, which was followed by a damping period to bring the rotor speed back to 1 pu. In contrast, both hybrid FCLs decelerated the rotor due to the resistive load on the machine from the HTS and switching limiters during the fault with lower deceleration in case of single-step FCL since it has the lowest impedance, as shown in Fig. 6(c). Nevertheless, both multistep configurations provided better damping performance since the voltage was built up to around 0.7 pu, which contributed to better power balance and enhanced angular stability [see Fig. 5(c)]. Switching signals were plotted as shown in Figs. 7 and 8. The phase voltage control scheme efficiently provided the switching

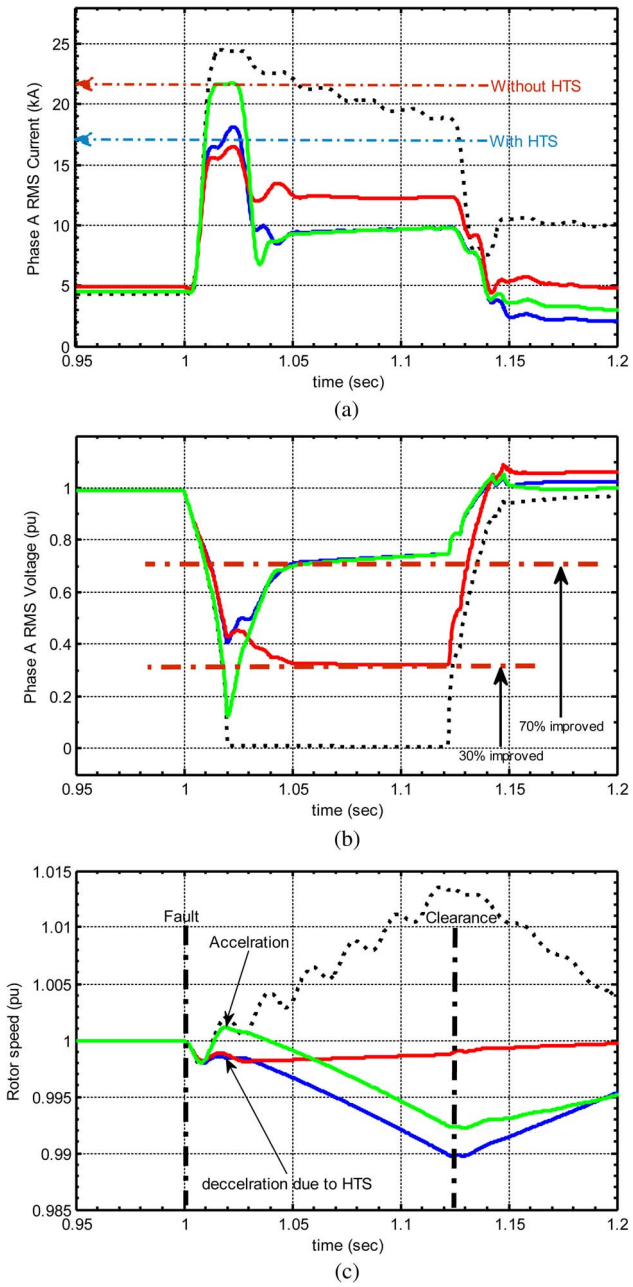

Fig. 6. Close view on phase-A signals.

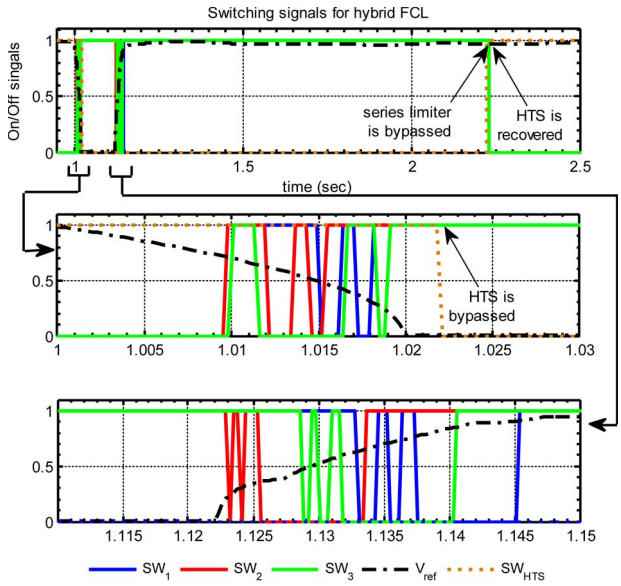

Fig. 7. Switching signals for hybrid FCL.

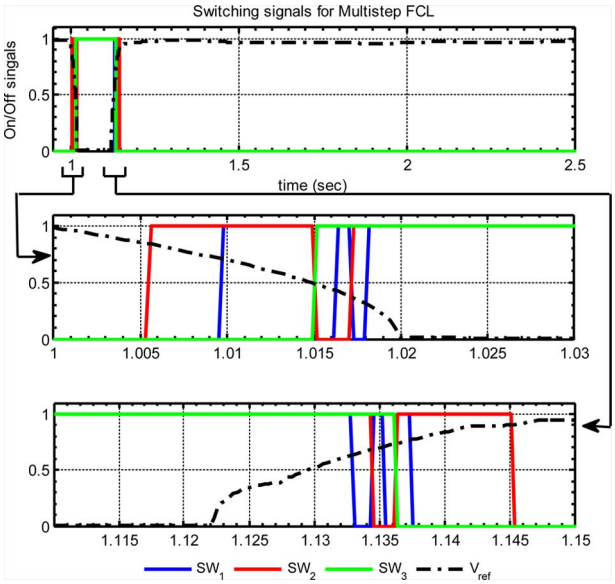

Fig. 8. Switching signals for multistep FCL.

signals according to V_{ref}, corresponding to the grid-side root mean square (RMS) voltage measurement. The switching operation suffers from two types of delays, which are the RMS calculation delay and the switching delay. Therefore, the HTS component is used to provide immediate response to cover these time delays, which are assumed to be 20 ms. Hence, the HTS is bypassed after this delay to start the recovery process. Meanwhile, the limiting resistors are still in service under the phase voltage-triggering scheme.

Once the fault is cleared, the limiter with the minimum resistance will remain in service to protect the system from faults until full HTS recovery is achieved according to the bypass scheme. The presence of this resistance loads the system and causes an overvoltage in an acceptable range by the grid operator, as shown in Fig. 5(b). According to test system characteristics and hybrid FCL design, results show a very minor overvoltage less than 1.1 pu, which is acceptable even in normal operating conditions and allows slower recovery superconductors to be utilized in this configuration. It also allows this scheme to utilize slower-response switches such as conventional breakers to be used for braking resistor switching.

B. Asymmetrical Fault Condition

The proposed multistep hybrid FCL scheme is designed to provide a per-phase compensation since HTS wires will respond in faulty phases only. Similarly, voltage-based and bypass triggering schemes are phase dependent. This gives the hybrid FCL capability to handle asymmetrical faults and mitigate the system unbalance. A double line-to-ground fault occurred between phases A and B for six cycles and caused around 80% voltage dip, as given in Fig. 9.

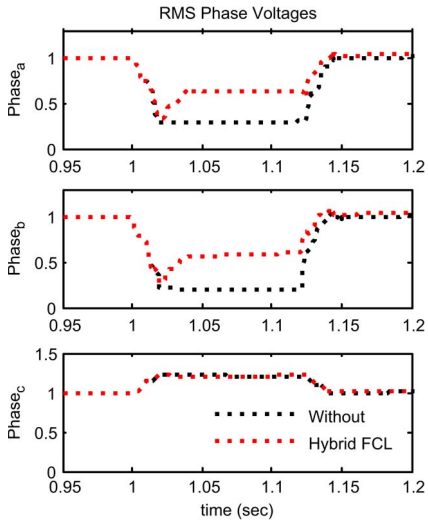

Fig. 9. Phase voltages during asymmetrical fault.

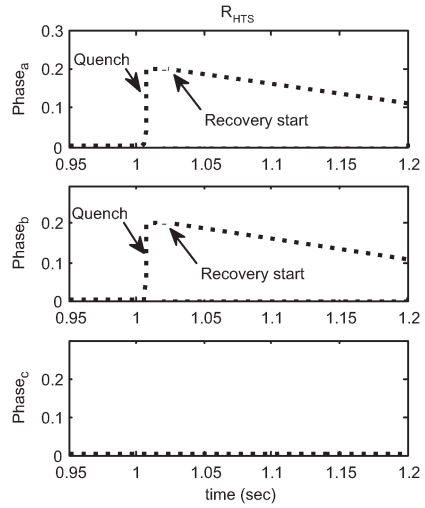

Fig. 10. HTS resistance during asymmetrical fault.

In response to this fault, superconductors at phases A and B quenched as shown in Fig. 10. Moreover, the switching signals are initiated from the voltage-based triggering scheme to these phases only. Phase-C limiters as well as HTS remained in nominal operation, as given in Figs. 10 and 11. This triggered action and superconductor's quench in the faulty phases resulted in an enhanced voltage profile as depicted in Fig. 9 with 40% improvement in the voltage of phases A and B, whereas the voltage at phase C remained the same.

V. Hybrid Operation Characteristics

The proposed combination of series-braking resistors and HTS-FCL demonstrated an enhanced performance and reliability to existing resistive-type HTS-FCLs. The hybrid HTS-FCL can be utilized for stability enhancement, adaptive voltage compensation, and fault-level mitigation. With regard to its main role as FCL, the hybrid FCL can overcome the issue of superconducting slow recovery by fast current transfer to series limiters (braking resistors), which not only allows early recovery to the HTS element but also limits the fault endurance requirement of the HTS since the HTS limiting action is required

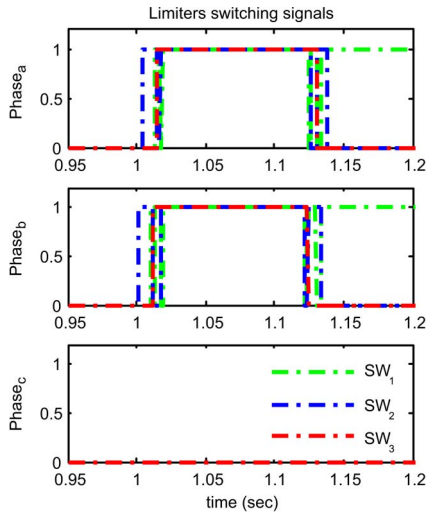

Fig. 11. Switching signals during asymmetrical fault.

only in the first few cycles. These lower HTS requirements can drop the cost and size of the superconductor and its associated cooling system compared with standard SFCL configurations. In contrast, this configuration requires multiple steps of series-braking resistors. Although it may increase the size and cost of the overall system, the presence of series limiters allows the hybrid FCL to provide an adaptive voltage compensation option, which is not achievable in conventional SFCLs and MFCL as well making it a reliable voltage booster and stabilizer scheme in comparison to available series compensation devices [27].

The hybrid FCL operation is also characterized by the type of switches used, which determine the overall response time. Preferably, solid-state switches should be used to minimize switching delays [28], keeping in mind that the acceptable response time should consider power system characteristics and HTS design (fault limiting capability and recovery time).

The use of such hybrid scheme is not limited to resistive-type HTS-FCLs; it can also be extended to inductive-type HTS-FCLs. In fact, the proposed voltage-based triggering scheme associated with series resistors can overcome stability drawbacks in an inductive FCL since they cannot dissipate the active power during disturbances, whereas series resistors can provide this type of operations in conjunction with the fault limitation from an inductive FCL.

VI. Conclusion

This paper has presented a hybrid series FCL configuration that combines a high-temperature superconductor with switched braking resistors. The proposed configuration relies on the fast quench of superconductors to provide a fast current limiting action and on the dynamic braking resistors to serve as voltage boosters. The use of braking resistors will lower the operation time of the superconductor to allow fast recovery. Moreover, the switched braking resistors will keep the system current level below the maximum fault-level interrupting limit of circuit breakers during the HTS recovery. The proposed configuration was tested using single- and multistep braking resistors in a single-machine-to-infinite-bus system. Results

demonstrated the superior performance of the proposed scheme in terms of fast fault mitigation, voltage recovery, and transient stability enhancement without deteriorating the system performance or violating its security constraints during the recovery process.

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