4M-6 (Invited)

# Packaging design considerations for mobile and Internet of things (IOT)

Piyush Gupta,
Qualcomm Inc,

**Abstract**

This talk will go over the various considerations that lead into final selection of a package for a particular application and end form factor. These aspects not only include cost and performance requirements but also include die constraints and OEM PCB choices. It will show an example that for different tier of phones; these trade-offs are different which leads to unique package selection choices. Than the talk will segue into system in package. Essentially highlighting how two unrelated trends of node shrinkage and end device form factor shrinkage are affecting package choices.

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## Introduction

There are mobile phones that sell all the way from $50 to $800. How do you design packages for such a wide range of cost points? This ultimately boils down to optimizing each solution for its own design point. For example the packaging choices made for a $50 phone means prioritizing cost over performance as opposed to designing for a $800 phone where one prioritizes performance over cost. These differing constraints lead to very different decisions not only for the type of the package type, the package size, the package pitch, but also the type of package capacitors. Other big factors that play into deciding the package is what are the OEM's ID constraints and Surface mount technology (SMT) constraints. Increasingly the OEMs are asking for a thinner phone and that means thinner package. The IC node that goes in the package adds some unique tradeoffs in terms of the first level interconnect geometry and hence the package substrate technology that goes with the IC.

## Processor package for mobile

This is normally the largest IC and the package in the system. Following are the key considerations when designing a processor package.

*A. DDR performance requirements.*

For a high tier phone, high DDR Bandwidth (BW) requirements mean high IO counts and unusually high DDR frequency. High frequency implies stringent Signal integrity requirements. This can usually only be met avoiding the PCB routing. Hence for this tier of phone POP becomes a natural choice. High IO requirements puts pressure on reducing the processor to the POP interconnect pitch. This leads to interposed based POP packages as shown in Figure 1.

For low tier phones the cost of eMCP is cheaper than POP, hence POPs are avoided. Instead non-POP based packages are used.

*B. Height*

Twin trends of thinner phones and larger battery requirements are leading to pushing the package height reductions.

This is leading to some innovative package choices such as embedded die packages as shown in Figure 2.

*C. OEM PCB technology choice*

Higher tier phones pay a premium for a smaller PCB area by increasing the PCB micro-via layers. For a higher tier phone OEM uses typically 3 or more micro-via layers. Hence the package pitch can be as less as 0.35mm. For a low tier phone OEMs typically use 1-2 micro via layers and relaxed PCB design rules. And hence the package pitch typically is between 0.4 - 0.5mm pitch. So even though the high tier phones require more interconnects on the PCB the fact that their package pitches can be less, means the package sizes for high tier and low tier phones are typically same size ie between 12x12 mm to 15x15 mm.

*C. Die Node*

We see most advance die nodes first introduced with flagship high tier phones. As nodes are shrinking from 28→16→14→10→7nm the level 1 interconnect density between IC and the package is shrinking. This leads to interesting level 1 interconnect technology choices. The trend is to move from solder bump to Copper pillar based Level 1 interconnects. Finer Level 1 interconnects puts pressure on the package substrate technologies to support fine Line width and spacing to as small as 10um/10um.

*C. Capacitors*

Again the highest tier phones demand most processing power from their CPUs and GPUs, leading towards ever increasing # of cores or Fmax requirements. This means constant evolution of the Power delivery requirement (PDN). So highest tier processor packages see package capacitors inside the substrate. For the capacitor also the trend is moving from Multi-layerd ceramic capacitor (MLCC) to silicon based capacitors. Silicon based



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capacitors provide the lowest self-inductances. Low tier phones typically avoid any capacitors to save cost.

*C. Other design considerations*

Since the low tier phones usually use inexpensive PCBs with one or no HDI layers, they can-not afford to have any cross routing in the PCB. Thus many times in order to map the processor IC interfaces to the other components in the phone, the # of layers in the packages are increased. Leading to cost increases in the package. This can be avoided by co-designing the IC and package and PCB all together.

**DRAM/Flash packages for mobile**

These are typically multi stack WB dies. They come in the following combinations. a) POP DRAM (LP4,LP4x) + discrete eMMC, UFS b) eMCP/uMCP with LP4x . As memory density requirements are increasing, the number of memory dies in a stack is increasing. Hence a major trend is how to avoid increasing the memory package height. So Memory Fanout (FO) is a trend in the packaging space for this.

**RF packages for mobile**

The RF packages are typically chosen as a wafer level package (WLP), quad flat lead (QFN) or a laminate based package. For RF packages the main considerations are IOs and die size. For low IO requirements WLP is the first choice. If the IOs are large than the choice boils down to lead based packages or laminate based packages. For high tier phones typically board space is a constraint. And since laminate based packages are smaller than QFN based packages for similar IOs, hence for high tier phones laminate-based packages are chosen.

**Power management packages**

PMIC packages design is a function of the # of power domains that need to be supported. As power management becomes more and more important, each power domain needs to be controlled separately. This means multiple bucks and lots of unique trace routing on the OEM PCB. Hence the first decision that needs to be made is the # of PMIC packages and their position on the PCB to avoid crossing of routed traces. After that the decision to select the package type is made. The main package choices are WLP or a FC package. This decision between WLP and FC mainly is driven by cost and supply chain availability rather than any major requirements. For highest tier phones there is typically a Thermal interface material (TIM) at the back along with a heat sink. But for a cheap phone there is no heat sink needed.

**IOT packages**

Packages for IOT face some unique challenges depending on the end device. For example for wearable's, board space and the power are even more of a constraint than the performance requirements as compared to a mobile space.

Another trend here is of ePOP (Flash+ DRAM both in a POP) packages. ePOP is unique to IOT due to low DRAM density requirements  space to put flash memory on the PCB.

Designing one chip and tooling many packages is also a prominent trend depending on the end user application. For example in wearable audio it may go to a ePOP sub 10x10 mm package vs in a home theatre it may go in a 21x21 mm 0.65mm pitch large package.

**System on chip (SOC) vs system in package (SIP )vs discrete packages**

The digital node shrink roadmap almost always precludes from SOC approach for digital and RF combined.

SIP approach is preferred when integration for miniaturization is desired over cost. When overall cost is optimized than usually discrete packages are cheaper. So for example smart watches SIP makes more sense, vs lets say a smart electric meter.

*A. Digital die size reduction*

As nodes shrink the IC size reduces, but the 2$^{nd}$ level of interconnect density does not reduce at the same scale. This implies there is free space inside the package. This could be used for putting some discrete chips as side by side in the package. Here the SIP becomes attractive as a means to save board space. Still SIP is desirable from cost point of view only  if each of the components require same number of layers in the combined package.

*B. Non-traditional IOT players*

There is an accelerating tend where non traditional companies with not much background in traditional phone design are asking for a integrated and certified end to end solution so that they can focus

on their strengths of IDs and fashion as a means of differentiation instead of investing in board design. This means that a system in package approach is very much needed. This means designing the RF+PMIC+processor packages together and selling it as a chipset.

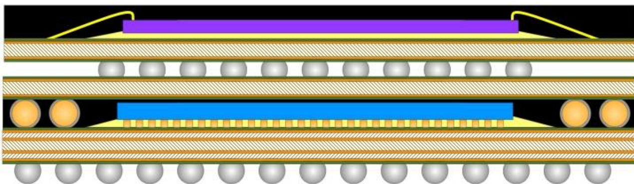

Fig. 1: Interposer based POP packages.

Fig. 2: Embedded die package

Fig. 3: 2 micro-via layer PCB

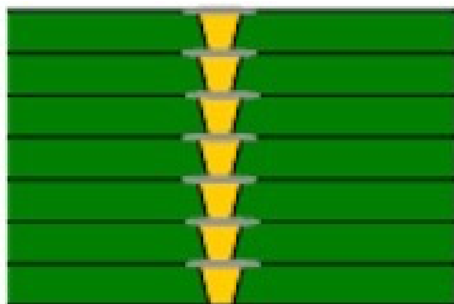

Fig. 4: 8 micro-via layer PCB