Adaptive and Intelligent Controller for Protection in Radial Distribution System

O.V. Gnana Swathika and S. Hemamalini

Abstract In this paper, a Field Programmable Gate Array (FPGA) based intelligent controller for overcurrent (OC) protection of a radial distribution system is realized. This controller monitors the radial distribution network continuously and when a fault is detected in the network, the FPGA based adaptive and intelligent controller performs the OC relay coordination and trips the appropriate circuit breakers of the system. The FPGA based digital prototype relay for overcurrent protection is realized with Atlys Digilent Spartan-6 FPGA kit. The performance of the FPGA based overcurrent protection technique for a 4-bus radial distribution system is compared with that of the conventional dual simplex algorithm. The proposed FPGA based overcurrent protection algorithm is also tested for an IEEE 33-bus radial distribution network.

Keywords Overcurrent relay · FPGA application · Radial distribution · Overcurrent protection

1 Introduction

Distribution Systems are the largest portion of the power system network that constitutes an array of radial feeders. The radial feeders of the distribution network are highly prone to faults, due to adverse weather conditions, equipment failure and accidents. A proper relay coordination technique helps to disconnect a minimum portion of the network and isolate the faulty part of the network using suitable overcurrent protection devices.

O.V. Gnana Swathika (✉) · S. Hemamalini
School of Electrical Engineering, VIT University, Chennai, India
e-mail: gnanaswathika.ov@vit.ac.in

S. Hemamalini
e-mail: hemamalini.s@vit.ac.in

H.A. Sulaiman et al. (eds.), *Advanced Computer and Communication Engineering Technology*, Lecture Notes in Electrical Engineering 362,
DOI 10.1007/978-3-319-24584-3_18

Fault location in the distribution system is highly complex due to uncertainty of load, phase unbalance, non-homogeneity of line and fault resistance [1]. Various research and working models are derived for accurate fault location in the distribution system in order to maintain high reliability factor of the system. The complexity level of the system keeps varying and thus a specific constrained algorithm is not sufficient to serve the purpose of fault identification. The measurement units are not widely deployed and are mostly limited to the substation; which in turn causes lack of monitoring and tracking the critical system data. At distribution level, there is always load inconsistency and thus there is a drastic variation in the number of generators that serve the network. The phase unbalance is predominant in radial distribution network. These are certain challenges faced in the process of fault identification. The basic process for the fault location incorporates voltage and current measurement blocks that facilitate the calculation of the impedance using the fundamental component [2] or harmonics [3]. An additional calculation burden like recalculation of the voltage and current at each node [2, 4, 5] is required for the compensation of the characteristics unique to the distribution system. A Fuzzy approach to identify the most possible fault location in a distribution system is suggested in [6]. It is necessary to identify the exact fault location instantaneously and take necessary actions to resume supply to customers quickly. This includes isolating the faulted section from the healthy section appropriately. To meet out the above requirements, Distribution Automation System (DAS) comes into play to efficiently perform fault handling. The most important counterpart for this system is the availability of reliable measurement database from SCADA systems. Distribution Automation (DA) analytical tools include various application functions [7, 8]. New algorithms were then deduced using Artificial Intelligence (AI) [9], wherein all the short circuit analysis is done offline, and the fault is located online faster than conventional methods.

Overcurrent protection is a protection scheme that a distribution system demands when there is short circuit or overload condition in the network. Transients in voltage or current may force a relay to mal-trip or fail-to-trip [10]. Frequently occurring switching transient data is updated in a database. The immunity of the relay to such transients is tested and developed. The key challenge in this scheme is to map all the switching transient data to the database. Reliability of a distribution system [11] is improved by locating and rectifying faults even before a crisis occurs by using intelligent distribution fault identification algorithms. In this, the distribution fault anticipation technique makes the distribution network to handle any stress that maybe caused due to increasing loads or bad environmental conditions. This technology has scalability issues due to reasons like huge data that is difficult to analyze. In [12] a central controller is used with communication to multiple measurement units of a realistic distribution system. Communication based digital relays identify high impedance faults in the network. This setup requires switching devices and relays on each feeder and is hence expensive. The overcurrent relay (OCR) is realized using DSP processor [13]. However, this method does not

provide accurate results, as no mathematical algorithms are involved. Fuzzy controller [14] is used to improve the performance of the overcurrent relay, but it is applicable only for medium voltage distribution networks. For optimum coordination of OCR, continuous genetic algorithm [15] is employed in a ring main system. The knowledge of the breaker operating time and coordination time interval is essential, without which this algorithm will not operate. The directional overcurrent coordination is analyzed for different topologies of the network and is solved using genetic algorithm [16]. OCR coordination for a distribution system with distributed generators is demonstrated using evolutionary algorithm [17]. The drawback of the algorithm is that the Time Multiplier Setting (TMS) variables of relays increase in complex network. Due to the unpredictable behavior of the distribution network, it is very crucial to identify the faulted section and isolate it from the healthy portion of the network quickly.

In this paper, an FPGA based intelligent controller with overcurrent protection capability for a distribution system is proposed. The intelligent controller monitors the various feeder currents of the system continuously. If any abnormality is identified in any section of the system, suitable OC relay coordination is employed immediately to ensure the safety of the network. The performance of the FPGA based controller is proved to be faster than the conventional Dual Simplex Method.

2 Directional Overcurrent (OC) Relay Coordination

The conventional overcurrent relay coordination algorithms are classified as trial and error method [18], topological analysis method [19, 20] and optimization method [21]. Dual simplex algorithm falls under the category of optimization method.

2.1 Problem Formulation

The directional OC relay coordination problem in a power system network is stated as an optimization problem, wherein the sum of the operating times of the relays in the system is minimized for near end fault. The objective function of the problem is given in (1).

$$\min z = \sum_{i=1}^{m} a_i TMS_i = \sum_{i=1}^{m} t_{i,i} \tag{1}$$

$$a_i = \frac{\lambda}{(PSM_i)^{\lambda} - 1} \tag{2}$$

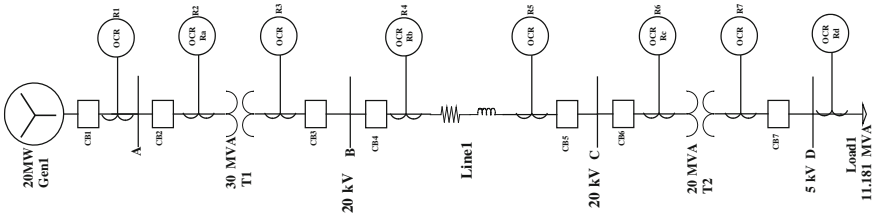

Fig. 1 4-bus radial distribution system

where

a_i	weight assigned for operating time of ith relay R_i
m	number of relays just beyond 'b' buses
TMS_i	Time Multiplier Setting of ith relay R_i
PSMi	Plug Setting Multiplier of ith relay R_i
λ	Constant of Relay
$t_{i,i}$	Operating time of primary relay at *i* for near end fault

The minimization problem is subjected to the following constraints:

(i) Coordination criteria

$$t_{b,i} - t_{i,i} \geq \Delta t \tag{3}$$

where

$t_{b,i}$	Operating time of backup relay for the same near end fault
Δt	Coordination time interval

(ii) Relay operating time

$$t_{i,i,max} \geq t_{i,i} \geq t_{i,i,min} \tag{4}$$

The dual simplex method is employed for optimum coordination of overcurrent relays in a radial test system [21, 22] using C programming. For the test system shown in Fig. 1, the normal IDMT relay with constants γ of 0.02 and λ of 0.14 are chosen. Minimum operating time for each relay is considered as 0.2 s and the coordination time interval (CTI) is taken as 0.3 s. The calculated values of a_i using (2) for the test system in Fig. 1 are shown in Table 1.

Table 1 Calculation of a_i

Fault position	Relay			
	R_a	R_b	R_c	R_d
Just beyond bus A	2.15	–	–	–
Just beyond bus B	2.77	2.15	–	–
Just beyond bus C	2.77	2.15	2.15	–
Just beyond bus D	1.75	1.47	1.47	2.15

2.2 Algorithm for Dual Simplex Method

1. Start.
2. Convert the minimization problem to maximization problem.
3. The greater than or equal to type constraints are converted to less than or equal to type constraints and surplus variables are added.
4. Create the dual simplex table by considering original variables as non-basics and slack variables as basics.
5. Form the cost coefficient ($C_j - \sum c_i \cdot e_{ij}$) row [22].
6. (a) Check if any element in this row is positive. If YES then go to step 13.
   (b) Check if all the elements in the row are non positive. If YES, then check if all the elements in the column of 'b' are non negative. If YES then optimal solution is reached. Go to step 12.
   (c) Check if all the elements in the row are non positive. If YES, then check if at least one element in the column of 'b' is negative. If YES then further optimization is possible. Go to step 7.
7. Identify the row which has the maximum negative value of b. This is considered as key row.
8. (a) There is no feasible solution for the problem, if all the coefficient values (aij) in key row are non negative. Now go to step 13.
   (b) If some a_{ij} in the key row are less than 0, then find the ratio for those columns:

$$\text{Ratio} = \left(C_j - \sum c_i \cdot e_{ij}\right) / \left(a_{ij}\right)$$

9. Identify the column having the smallest (positive) ratio. This is considered as the key column.
10. Identify the pivot element by mapping the key column and key row. Start the formation of next dual simplex table.
11. Go to step 5.
12. Print results.
13. Stop.

3 Proposed FPGA Based Adaptive and Intelligent Protection Control

In this paper, FPGA based adaptive and intelligent protection controller is developed to efficiently provide overcurrent protection for a radial distribution network. FPGA constitutes an array of configurable logic blocks, I/O Blocks and Block RAMs. The configurable logic block (CLB) contains slices. Each slice contains

look-up tables (LUT), carry and control logic and registers. These slices are used independently or together for wider logic functions. There are buffers associated with each CLB, which are accessed by all the outputs of a CLB.

In FPGA based systems, signal processing functions are implemented with higher degree of freedom and low cost. Moreover they are easily reprogrammable for any changes in the functionality [23]. This eliminates the redesigning costs. While contrasting FPGA with microprocessor or DSP, the performance of FPGA is not tied to the clock rate. Thus highly parallel structures are easily constructed for processing data using FPGA [24]. The FPGA based systems perform at higher speed when compared with Microcontroller or DSP counterparts. Due to these predominant features, FPGA based systems are currently employed to perform power flow monitoring, fault identification [25] and protection in complex distribution systems. The power flow data of a power system network are transmitted to FPGA using wireless data monitoring cards [26]. To handle huge data from the network, more number of channels with higher sampling rate is required. Hence, FlexRIO is incorporated for data acquisition and real time data processing [27]. Due to the above features, FPGA devices are used in control platforms in various real time applications such as wireless telecommunications, image and signal processing, robotics and renewable energy systems [28].

Adaptivity of relays in a radial distribution system enables the protective system to act in accordance with the upcoming events. The proposed FPGA based adaptive controller performs two functions. The primary function is to perform fault monitoring, where the time stamped current data from all the feeders of the test system are captured and fed to the central protection center. The second function is to perform fault handling i.e. once a fault is identified in a feeder segment, relay coordination is done to isolate the faulted section from the healthy portion of the radial distribution network.

The directional overcurrent relay is employed in the radial distribution system for overcurrent protection. The normal current in all the feeders of the system are calculated to fix the CT ratio in all the feeders. The threshold current is computed using (5).

$$Threshold\ Current = \frac{Full\ Load\ Current\ in\ a\ Specific\ Feeder}{CT\ Secondary\ Current} \tag{5}$$

The current sensors are deployed at all feeders of the radial distribution network to sense the current that flows in that feeder at any instant of time. In the test system shown in Fig. 1, current sensor is placed in each feeder segment. These currents are captured continuously into a text file in the PC. The purpose of the controller is to monitor these feeder currents by reading the text file and comparing them with their respective threshold currents to ensure that they do not exceed the permissible current limit. If the current sensed in each feeder of the radial system is not more than their respective threshold current, the system is said to be in the normal state. If the above condition is violated, then the system is said to be in faulted state. The

time of operation for the relays placed in the respective feeders is dynamically calculated using (6–9).

$$Pick-up\ current = Setting\ from\ relay\ catalogue * CT\ phase\ current \tag{6}$$

$$Time\ Multiplier\ Setting(TMS) = Setting\ as\ per\ relay\ catalogue \tag{7}$$

$$Current\ setting(CS) = \frac{Fault\ Current(IF)}{(1.5 * Pick-up\ current)} \tag{8}$$

$$Time\ of\ operation\ of\ relay = \frac{0.14 * TMS}{[(IF/CS)0.02 - 1]} \tag{9}$$

In the faulted state, the fault indicator available within the intelligent overcurrent protection center immediately indicates the abnormal behavior of the system. The faulted feeder details are transmitted through the Universal Asynchronous Receiver and Transmitter (UART) and displayed on the HyperTerminal running on the PC. If the fault in that feeder is not cleared within a stipulated amount of time (9), then the backup protection comes into play.

4 Results and Discussion

For the 4-bus radial distribution test system shown in Fig. 1, a FPGA based intelligent overcurrent protection controller is designed. Normal Inverse Overcurrent Relays (OCR) [29] R1 through R7 and CTs are fixed at seven feeders starting from upstream to downstream. Both current and time grading are assumed. This test system is subjected to load flow analysis. Feeders Gen1-A, A-T1, T1-B, B-line1, Line1-C, C-T2 and T2-Load1 have 8-bit digital equivalent current signals notated as *isa, iat1, it1b, ibm, imc, ict2 and it2l* respectively.

4.1 Test System Monitoring and Feeder Current Extraction

The feeder currents are periodically captured in a text file. The normal current in various feeder segments are listed in Table 2. In Gen1-A feeder, the full load current is 0.5672 kA. Hence a 600/5 CT is used in Gen1-A feeder. Similarly the CT's are fixed for the remaining feeders.

The threshold current for all the feeders of the 4-bus systems are tabulated in Table 3. A three-phase fault is initiated in the test system between T2 and Load. The fault currents in the various feeders are as shown in Table 2. Once the feeder current exceeds the threshold current shown in Table 3, the relay coordination ensures

Table 2 Normal and 3-phase fault current in a 4-bus radial system

Line segment	Normal current, kA	Fault current, kA
Gen1-A	0.5672	2.808
A-T1	0.2836	2.808
B-C	0.2836	1.404
C-D	1.1345	5.616

Table 3 Threshold current for relays

Relay number	Threshold current (rms), A
R1	120
R2	120
R3	60
R4	60
R5	60
R6	60
R7	240

which relay should trip to isolate the faulted section from the healthy portion of the network.

4.2 FPGA Based Intelligent Overcurrent Protection Controller

The FPGA based overcurrent protection scheme is implemented using Atlys circuit board which is a complete, ready-to-use digital circuit development platform based on a Xilinx Spartan-6 LX45 FPGA with speed grade of minus 3. The Spartan-6 LX45 is optimized for high-performance logic. It has 6822 slices, each of which contains four numbers of 6 input LUTs and eight flip-flops. The memory specification is 2.1 Mbits of fast block RAM. 58 DSP slices are also available. The clock speed is 500 MHz+. The VHDL modules used for the implementation of the OCR coordination algorithm are as shown in Fig. 2.

4.2.1 Overcurrent Relay Coordination Algorithm

Text_read.vhd

The purpose of text_read.vhd module is to read the text file located in the PC into the FPGA kit. This file contains the values of all feeder currents of the test system at any instant of time. As there are 7 feeder segments, 7 set of feeder currents will be available in that file. The output of this VHDL file is labeled as dataout (0:6) which represent the 7 individual instantaneous feeder currents. Each dataout port is an 8-bit value.

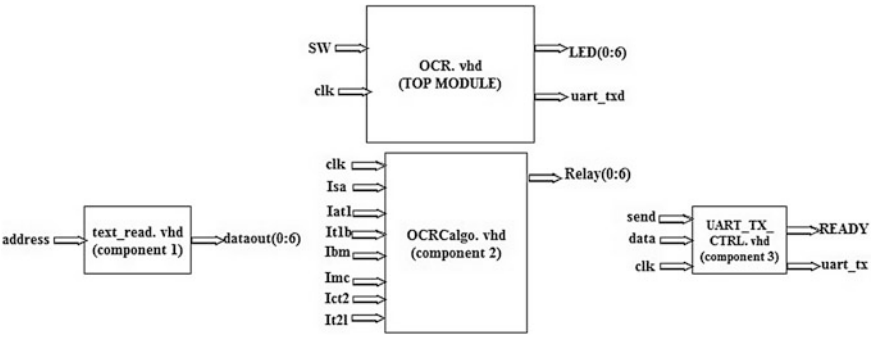

Fig. 2 VHDL modules for OCR coordination algorithm

OCRCalgo.vhd

The input to OCRCalgo.vhd module are the feeder currents namely isa, iat1, it1b, ibm, imc, ict2 and it2l, along with the clk signal. Dataout (0:6) are mapped to these currents. This module is responsible for identifying if there is an OC fault in the feeder and also to trip the appropriate circuit breakers taking into account the calculated time of operation of individual relays. Hence the primary and backup protection is triggered from this block in the event of occurrence of OC fault. The output of this relay is connected to the associated breakers of individual relays R1 through R7.

UART_TX_CTRL.vhd

The Atlys kit includes an EXAR USB-UART bridge to allow PC applications to communicate with the board using a COM port. UART onboard of the FPGA kit is used to establish asynchronous serial communication. The UART serial module has three sub-modules: the baud rate generator, receiver module and transmitter module. The local clock signal is provided by the baud rate generator. Once the baud-rate is fixed, both the transmitter and the receiver's internal clock are set to the same frequency. The UART receiver module enables the reception of serial signals at RXD and converts them into their respective parallel data. The UART transmit module with the help of frame format converts the data bytes into serial bits and transmits those bits through TXD. The UART_TX_CTRL.vhd module contains three input ports namely 'send', 'data' and 'clk'. The two output ports are 'READY' and 'uart_tx'. The string definition is such that the values stored at each index are the ASCII values of the indicated character [30]. This module is used to display the string, which is the error message indicating details of faulted feeder, on the HyperTerminal.

OCR.vhd

OCR.vhd is the top module which has three components namely Text_read.vhd, OCRCalgo.vhd, UART_TX_CTRL.vhd which are mapped to it. SW and clk serve as inputs to this top VHDL module. LED (0:6) and uart_txd are the outputs of this

module. The user constraint file pins.ucf is associated with the top module at the implementation stage. This file matches equally named nets to equally named constraints. Since there are 7 feeders, 7 LEDs are rigged up in the kit. When SW = 1, the OCR coordination algorithm is triggered for the network that is being monitored. The UART_TXD is connected to UART port of the kit, which communicates with the HyperTerminal in PC. In order to incorporate the appropriate time of operation for relays R1 through R7, the clock of 96 MHz is utilized.

4.2.2 Procedure to Perform the OCR Coordination Using FPGA Kit

Make the connections and simulate the top module namely OCR.vhd. If a fault is initiated in the feeder T2-Load1, the simulated output for the relay coordination using FPGA is as shown in Fig. 3. The plot indicates that the relay operating time strictly follows the time of operation given in Table 4. The time of operation of the upstream relay is 2.9 ms. Double click on HyperTerminal and give a name for the new connection. Identify the COM port to which the FPGA kits' UART port is connected. Select that COM port detail in the dropdown menu. Click on CONFIGURE and set the following parameters: Bits per second: 9600; Data bits: 8; Parity: None; Stop bits: 1; Flow Control: None. The HyperTerminal is now ready to use. Synthesize and implement the top module OCR.vhd. Double click on Generate Programming file and this will generate the appropriate.bit file. Double click on "Configure Target Device". This triggers the IMPACT software to open. Double click on Boundary Scan. Right Click and select "Initialize Chain" and establish the connection between the PC and the FPGA kit. Assign the.bit file to the FPGA kit and thereby dump the bit file on the FPGA. If faulted feeder is T2L and if SW = 0, the fault in the feeder is indicated by glowing the appropriate LED. In this example

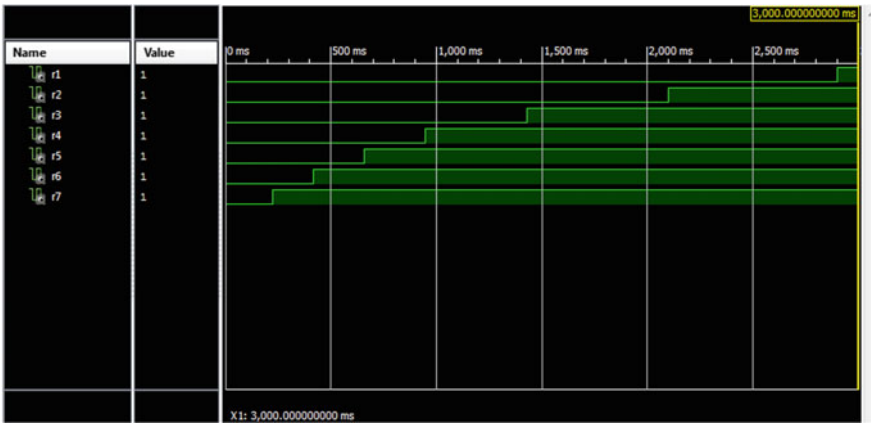

Fig. 3 FPGA based relay coordination 4-bus radial distribution system

Table 4 Time of operation set for the relays

Relay number	Time of operation, ms
R1	2900
R2	2100
R3	1430
R4	947
R5	660
R6	418
R7	223

LED6 associated with Relay 7 (downstream relay) will glow. If faulted feeder is T2L and if SW = 1, the OCR coordination algorithm will be triggered. The faulted feeder details are displayed on the HyperTerminal as:

"OC Fault in Feeder t2l"

LED6 glows to indicate fault in feeder T2L. If the fault is uncleared i.e. if the circuit breaker associated with R7 does not trip within the stipulated time of operation, then LED6 continues to glow and LED5 glows to indicate that backup protection is enabled in the network. This procedure continues from downstream to upstream until the fault is cleared as shown in Fig. 4.

An IEEE-33 bus system shown in Fig. 5 is considered for analysis. Let r_{i_j} indicate the relay notation for a relay placed between bus i and bus j. For a fault initiated in feeder connecting bus 31 and bus 32, the FPGA based overcurrent relay coordination is as shown in Fig. 6. The time of operation for the upstream relay in

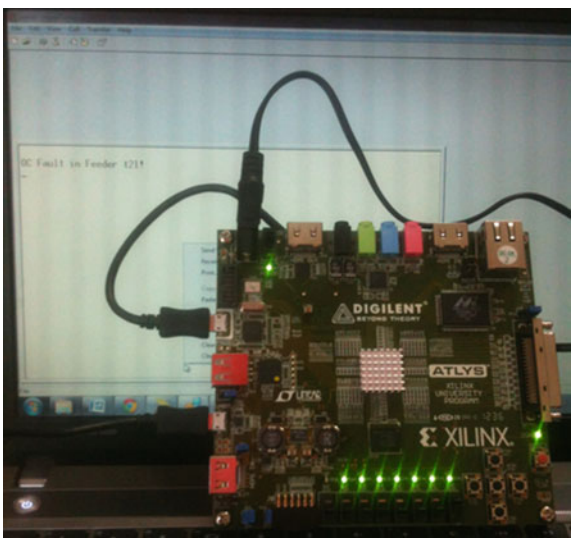

Fig. 4 FPGA based intelligent protection control system for 4-bus radial distribution system

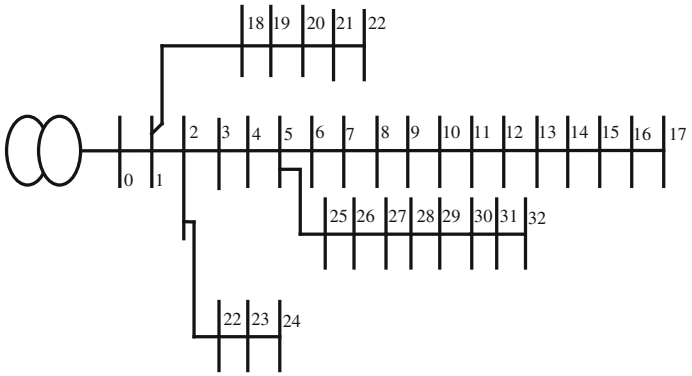

Fig. 5 IEEE 33-bus radial distribution system

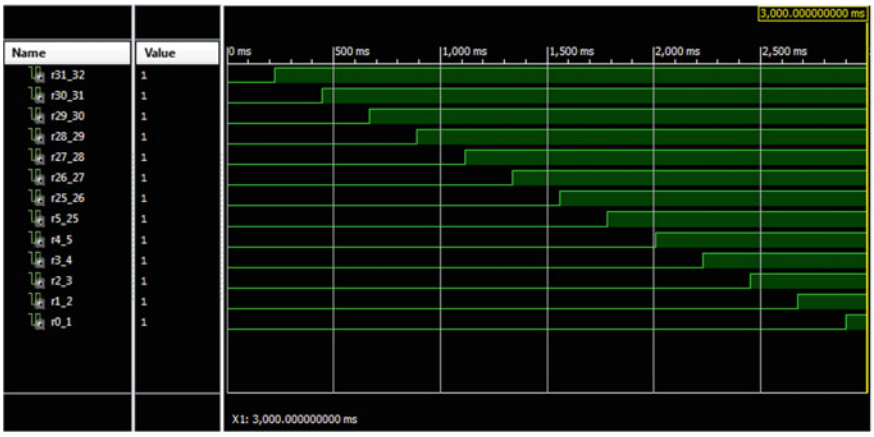

Fig. 6 FPGA based intelligent protection control system for the IEEE 33-bus radial distribution system

the FPGA based overcurrent relay coordination for the 4-bus and 33-bus system is at 2.9 s; whereas it is 3.1 s using conventional algorithms.

The resources used for the FPGA implementation of the overcurrent protection system for the 4-bus test system is shown in Table 5. Table 6 compares the time of operation of upstream relay for the 4-bus radial system for both FPGA based and conventional dual simplex based directional OC relay coordination [31, 32]. It is observed that there is a significant improvement in speed of clearing the fault, using the FPGA based adaptive and intelligent protection control system in comparison with the conventional algorithms for directional OC relay coordination. This algorithm is applicable to any complex distribution system and requires almost same number of bonded IOBs irrespective of the size of the network.

Table 5 Device utilization summary

FPGA resources	Used	Available	Utilization (%)
Number of slice register	181	54576	1
Number of slice LUTs	623	27288	2
Number of occupied slices	207	6822	3
Number of MUXCYs used	456	13644	3
Number of bonded IOBs	10	218	4

Table 6 Time of operation analysis

Time of operation (s)	FPGA based directional OC relay coordination	Dual simplex algorithm based directional OC relay coordination
	2.9	3.453

5 Conclusion

The proposed adaptive and intelligent protection control system is realized using FPGA technology. The FPGA based system identifies the fault instantly on the test system and appropriate OC relay coordination technique is applied to isolate the faulted section of the network from the healthy portion. The overcurrent relay coordination is completely centralized and based on the state-of-the-art technology. The FPGA based directional overcurrent relay coordination is proved to be faster than conventional optimization technique like Dual Simplex Method. This work maybe enhanced and implemented in large complex distribution systems with renewable energy sources.

Appendix

Generator (Gen1): 20 MW, 25MVA, 10 kV
Transformer (T1): 10 kV/20 kV, 30 MVA
Line Impedance: 2 + j4 Ω
Transformer (T2): 20 kV/5 kV, 20 MVA
Load1: 10 MW, 5 kV, 11.181 MVA

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