A Colpitts CMOS Quadrature VCO Using Direct Connection of Substrates for Coupling

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***Abstract*—A new low-phase noise low-power quadrature voltage-controlled oscillator (QVCO) using differential Colpitts oscillator is presented. The proposed QVCO is composed of two identical current-switching differential Colpitts VCOs in which the first core VCO is coupled to the second in an *in-phase* manner, and the second core VCO is coupled to the first in an *anti-phase* manner. To couple the two core VCOs, the substrates of the cross-connected transistors as well as the substrates of MOS varactors are used; alleviating the need for any extra elements for coupling, which could add noise and increase power dissipation. A linear (sinusoidal) analysis is presented that confirms that the proposed circuit generates quadrature waveforms. The proposed coupling technique can be generalized to *N* differential Colpitts VCOs for multiphase signals generation.**

***Index Terms*—Current-switching Colpitts-oscillator, low-phase noise, multiphase, quadrature oscillator.**

I. Introduction

Quadrature and multiphase voltage-controlled oscillators are indispensable key building blocks in many modern transceiver front-ends, whose performance can significantly affect the overall performance of the communication system.

Different techniques for quadrature signal generation are available [1]. Injection-locked LC quadrature voltage-controlled oscillators (LC-QVCOs) based on first-harmonics [2], [3] and super-harmonics [4], [5] injection have become widely popular in RF circuits because of their good phase noise.

LC-QVCOs have two main parts: a pair of identical LC-VCOs and a coupling network, both of which contribute to the overall QVCO phase noise performance. To improve the phase noise in previously reported LC-QVCOs, efforts were mostly focused on improving the coupling network utilizing a variety of active [2], [3] or passive [4], [5] coupling circuits, while the core VCO stayed almost invariably the cross-connected type.

In conventional cross-connected LC-VCOs, the noise generated by the active components perturbs the VCO outputs at their zero crossings, i.e., the maximum noise sensitivity point [6]. On the other hand, in Colpitts oscillators, the maximum noise level, i.e., the maximum of the impulse sensitivity function [6], generated by the core transistors is aligned with the minimum oscillator sensitivity points. Thus, as shown in [6], Colpitts oscillators have superior cyclostationary noise properties and as such, potentially, a better phase noise performance compared to the conventional cross-connected LC-VCOs.

In recently reported QVCOs, differential Colpitts oscillators have replaced the cross-connected oscillators, thus achieving a lower phase noise [7]–[14]. In [11] two complementary Colpitts VCOs are coupled to each other via four parallel coupling transistors. However, parallel transistors dissipate power and can degrade the phase noise of the QVCO. To reduce the effect of noise of the coupling transistors, a configuration known as noise-degenerated has been proposed where the coupling transistors are placed in series with core transistors [8]. While the phase noise and power consumption are reduced, stacking of transistors limits the voltage headroom. In the QVCO reported in [13] and [14], passive elements are used instead of active coupling devices.

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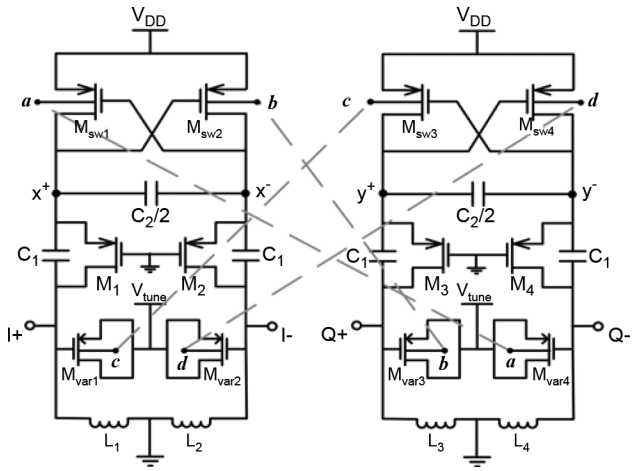

Fig. 1. Schematic of the proposed quadrature VCO.

In all the above proposed Colpitts QVCOs extra devices are used for coupling, which can degrade the overall performance of the QVCO and increase the chip area. Furthermore, any mismatches between coupling devices may disturb the symmetry of the circuit, leading to phase error.

This work presents a new low-phase noise low-power quadrature voltage-controlled oscillator in which two identical current-switching differential Colpitts VCOs are coupled without extra coupling devices that could potentially degrade the phase noise and power consumption.

The proposed QVCO and its analysis are given in the next section. Simulation results and a comparison of its operation with previously reported QVCOs are presented in Section III. Conclusions are drawn in Section IV.

II. Analysis of the Proposed QVCO

The proposed quadrature VCO is shown in Fig. 1. The circuit is comprised of two identical switching differential Colpitts VCOs which are coupled in an "in-phase anti-phase" scheme. As shown in Fig. 1, no coupling devices are added, and thus no extra sources of noise and power consumption are introduced.

As illustrated in Fig. 1 the bulks of the switching transistors (nodes a and b of $\mathrm{M_{sw1,2}}$) of the first core VCO are connected to the bulks of the MOS varactors (nodes a and b of $\mathrm{M_{var3,4}}$) of the second core VCO in an "anti-phase" manner, and the bulks of the switching transistors (nodes c and d of $\mathrm{M_{sw3,4}}$) of the second core VCO are connected in an "in-phase" manner to the bulks of the MOS varactors (nodes c and d of $\mathrm{M_{var1,2}}$) of the first core VCO. Since in a technology with P-type wafer the PMOSFETs are placed in separate wells, their bulks can be connected to different potentials. Thus, by choosing the switching transistors and MOS varactors as P-type, there is no need for the use of the triple-well technology option.

It should be noted that the substrates of the MOSFETs in this circuit are not in a floating state. The substrate potential is fixed by the circuit comprised of V_{DD}, source-substrate diodes in $\mathrm{M_{sw}}s$, the substrate-source/drain diodes in $\mathrm{M_{var}}s$ and V_{tune}. This potential, however, is not as well regulated as V_{DD} and as such, for the purpose of reducing the effects of substrate noise on the phase noise, use of layout techniques such as Guard ring is recommended. In addition, in the circuit the potential at nodes a, b, c, and d can be set at any particular value by connecting them to a desired potential via four resistors.

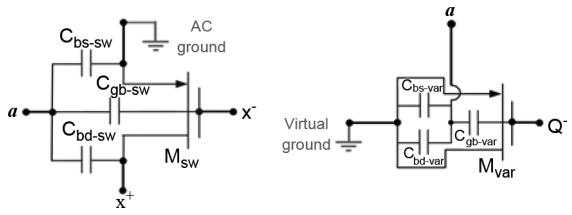

Fig. 2. Intrinsic capacitances that play the role of coupling elements.

The main idea in the proposed QVCO is to use the intrinsic capacitances of the core VCO's transistors instead of any extra coupling elements. As shown in Fig. 2, the gate-bulk and the bulk-drain capacitances of the switching transistors, and the gate-bulk capacitances of the MOS varactors play the role of coupling devices and provide the injection path for coupling signals, thus eliminating the need for any extra AC coupling capacitors and DC biasing resistors [14]. Furthermore, to reduce the noise contribution of the core VCOs to the overall phase noise, the noise-wise superior Colpitts structure replaces the conventional cross-connected LC-VCOs.

To show that a 90° phase difference exists between the outputs of the proposed circuit, i.e., $I^{\pm}$ and $Q^{\pm}$ in Fig. 1 are in quadrature, a linear analysis is presented as follows. In this analysis it is assumed that the waveforms are sinusoidal.

Due to the symmetry of the proposed circuit in Fig. 1 the amplitude of all output voltages (i.e., $I^{\pm}$ and $Q^{\pm}$) are equal. Because of the differential structure of the core VCOs, there is a 180° phase difference between the potentials of the nodes I^+ and I^- (and also between those of Q^+ and Q^-). The potentials at nodes I^+ and Q^+ are denoted with V and $Ve^{j\phi}$ in phasor domain, respectively, with V being the voltage amplitude and ϕ the phase difference between potentials of I^+ and Q^+ (also between potentials of I^- and Q^-). Applying KCL at nodes a and d, following can be written (nodes $V_{\rm tune}$ and $V_{\rm DD}$ are virtual ground in Figs. 1 and 2):

$$\begin{aligned} &j\omega C_{bs-sw}V_a + j\omega C_{gb-sw}(V_a - V_{x^-}) + j\omega C_{bd-sw}(V_a - V_{x^+}) \\ &+ j\omega(C_{bd-\rm var} + C_{bs-\rm var})V_a + j\omega C_{gb-\rm var}(V_a + Ve^{j\phi}) = 0 \end{aligned} \quad (1)$$

$$\begin{aligned} &j\omega C_{bs-sw}V_d + j\omega C_{gb-sw}(V_d - V_{y^+}) + j\omega C_{bd-sw}(V_d - V_{y^-}) \\ &+ j\omega(C_{bd-\rm var} + C_{bs-\rm var})V_d + j\omega C_{gb-\rm var}(V_d + V) = 0 \end{aligned} \quad (2)$$

where V_a and V_d are the phasors of the voltages at nodes a and d, and C_{gb}, C_{bs}, and C_{bd} are the intrinsic gate-bulk, bulk-source and bulk-drain capacitances of the transistors, respectively. Also, the potentials at nodes x and y are denoted with V_x and V_y in phasor domain.

Since the transistors $\rm M_{1-4}$ act as common-gate amplifiers, the voltage of the drain of this transistors (i.e., $I^{\pm}$ and $Q^{\pm}$) are amplified versions of their source potentials (i.e., $x^{\pm}$ and $y^{\pm}$). Suppose that the voltage gain of the common-gate amplifiers are denoted by $A_v (A_v > 0)$, then V_{x+} and V_{y+} can be replaced with V/A_v and $Ve^{j\phi}/A_v$, respectively. Therefore (1) and (2) can be rewritten as

$$\begin{aligned} &j\omega V_a(C_{bs-sw} + C_{gb-sw} + C_{bd-sw} + C_{bd-\rm var} + C_{bs-\rm var} + C_{gb-\rm var}) \\ &= -j\omega\frac{V}{A_v}(C_{gb-sw} - C_{bd-sw} + A_v(\cos\phi + j\sin\phi)C_{gb-\rm var}) \end{aligned} \quad (3)$$

TABLE I
CIRCUIT PARAMETER VALUES OF THE PROPOSED QVCO USED FOR SIMULATIONS (R_L IS THE OHMIC LOSS OF INDUCTORS)

Parameter	Value	Parameter	Value
$(W/L)_{Msw}$	38 µm/0.18 µm	C_1	1 pF
$(W/L)_{M1-4}$	22 µm/0.18 µm	C_2	0.5 pF
$(W/L)_{Mvar}$	300 µm/0.18 µm	V_{dd}	1.8 volt
L	1 nH	V_{tune}	0.85 volt
r_L	1 Ω		

$$\begin{aligned} &j\omega V_d(C_{bs-sw} + C_{gb-sw} + C_{bd-sw} + C_{bd-\rm var} + C_{bs-\rm var} + C_{gb-\rm var}) \\ &= j\omega\frac{V}{A_v}((\cos\phi + j\sin\phi)(C_{gb-sw} - C_{bd-sw}) - A_v C_{gb-\rm var}). \end{aligned} \quad (4)$$

Due to the symmetry of the circuit, the amplitude of the voltages at nodes a, b, c, and d are the same, i.e., $|V_a| = |V_d|$. Therefore the absolute values of the left-hand side of (3) and (4), and thus the absolute values of their right-hand side are equal, as expressed in (5) at the bottom of the page. Solving (5) to find ϕ, gives

$$\phi = k\pi + \frac{\pi}{2} \quad k = 0, 1, 2, \ldots \quad (6)$$

indicating that outputs are in quadrature. At this point it is worth mentioning that, while occurrence of both possible order of phases, i.e., potential at I^+ *leading* or *lagging* that of Q^+, have been reported in literatures (and (6) also shows the same thing), numerous simulations performed in this work always showed a unique order of phases, i.e., potential at Q^+ always leaded that of I^+. Another point to be mentioned is that, although the above analysis was based on sinusoidal waveforms, simulations showed that even for non-sinusoidal waveforms which could result from the low quality factor of the tank circuit, the proposed QVCO still does generate robust quadrature outputs.

In this circuit, coupling factor K_c is defined as the ratio of coupling current to switching current i.e., $K_c = I_{cp}/I_{sw} = (G_{sb}V_a)/(G_{sw}V_x^-) = A_v.A_{var}(G_{sb}/G_{sw})$, where G_{sb} and G_{sw} are the effective large signal transconductance for the source-bulk and gate-source of the switching transistors $M_{\rm sw}$, and $A_{\rm var}$ is the ratio of V_a/V_Q^- (e.g., simulation showed that A_v and $A_{\rm var}$ were about 8 and 0.1, respectively, for circuit parameters in Table I). While in a small signal region the term G_{sb}/G_{sw} is almost constant for a particular technology, the desired coupling factor can be realized by changing the voltage gain A_v, *i.e., changing the size of* M_{1-4} *and ratio of* C_1 *and* C_2.

III. SIMULATION RESULTS

The proposed quadrature Colpitts VCO is designed and simulated in a standard 0.18-μm RF-CMOS technology. The performance is compared to recently reported QVCOs. Agilent ADS is used for simulations. Fig. 3 shows the simulated waveforms using the circuit parameter values shown in Table I. The ohmic loss of each inductor was modeled as a series resistor (r_L) with 1Ω per each nH of inductance [9]. Since no extra devices were used for coupling, no parasitic element is imposed on the tank circuit resulting in a wide tuning range. According to simulations, oscillation frequency varies from 4.95 to 5.92 GHz when $V_{\rm tune}$ is swept from 0 to 1.8 V, resulting in a tuning range of 18%, as shown

$$\begin{aligned} &\sqrt{((C_{gb-sw} - C_{bd-sw}) + A_v C_{gb-\rm var}\cos\phi)^2 + (A_v C_{gb-\rm var}\sin\phi)^2} \\ &= \sqrt{((C_{gb-sw} - C_{bd-sw})\cos\phi - A_v C_{gb-\rm var})^2 + ((C_{gb-sw} - C_{bd-sw})\sin\phi)^2}. \end{aligned} \quad (5)$$

TABLE II
PERFORMANCE SPECIFICATIONS OF SOME PREVIOUSLY REPORTED AND THE PROPOSED QVCO (POST-LAYOYT SIMULATION IS USED FOR THIS WORK)

QVCO	Extracted data	Technology [μm]	f_{osc} [GHz]	P_{QVCO} [mW]	S_{SSB} (Phase-noise) [dBc/Hz]	Tuning range	Phase error	*FOM* [dB]	FOM_T [dB]
[11]	Measurement	0.25	2.62	12.34	-116.03 [@1MHz]	21.8%	3.34°	-173.4	-183.8
[13]	Measurement	0.18	4.5	3.96	-115 [@1MHz]	11%	N/A	-182.2	-190.1
[7]	Measurement	0.18	4.8	12.6	-120 [@1MHz]	6.25%	N/A	-182.5	-189
[9]	Measurement	0.18	2.33	14.4	-130.4 [@3MHz]	12%	N/A	-176.5	-187.3
[10]	Measurement	0.18	5.44	9.9	-124.36 [@1MHz]	4%	0.73°	-189.1	-195
This work	**Post-layout simulation**	**0.18**	**5.35**	**8**	**-138.9 [@3MHz]** **-128.7 [@1MHz]**	**18%**	**0.45°**	**-194.8** **-194.2**	**-204.8** **-204.2**

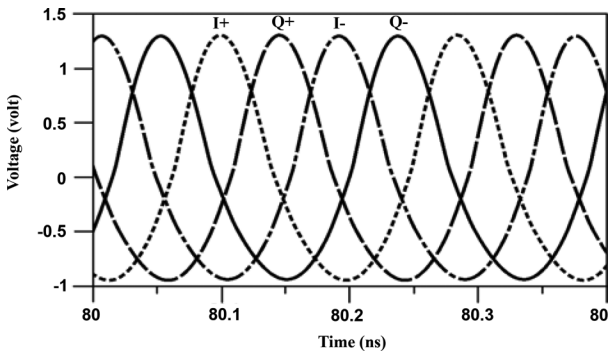

Fig. 3. Output waveforms of the proposed QVCO.

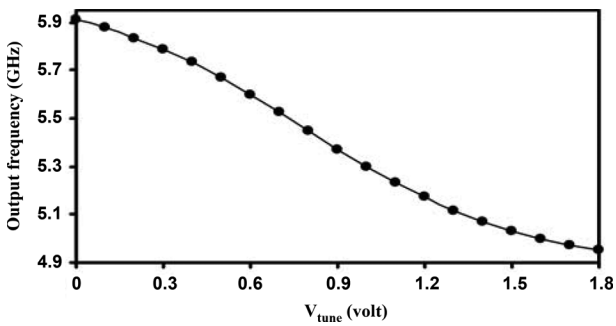

Fig. 4. Simulated frequency tuning range of the proposed QVCO.

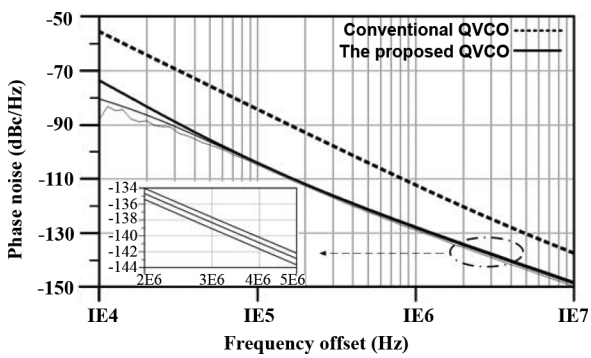

Fig. 5. Simulated phase noise of the proposed QVCO (for different coupling factors) and that of P-QVCO with coupling technique proposed in [11].

in Fig. 4. The total dc current drawn from a 1.8-V power supply is 4.44 mA leading to 8 mW total power consumption.

The simulated phase noise of the proposed Quadrature VCO at 5.4 GHz center frequency is compared to that of [11] in Fig. 5. For the purpose of this simulation, the parameters of each circuit are chosen such that both have the same oscillation frequency and power dissipation (the coupling technique proposed in [11] was utilized and simulated in 0.18-μm CMOS technology).

As expected, the phase noise in the proposed circuit is significantly improved, which is the result of elimination of the extra coupling devices and their associated noise sources and also the use of Colpitts VCO instead of conventional LC-VCO. As Shown in Fig. 5, changing the coupling factor will result in change in the phase noise [3]. However Monte Carlo analysis shows no degradation of phase accuracy due to change of coupling factor.

A comparison of the performance of the proposed QVCO with those of the previously reported QVCOs is presented in Table II, using the following figure of merit (FOM) [3]:

$$\mathrm{FOM} = 10\log\left(S_{\mathrm{SSB}}\left(\frac{\Delta f}{f_{\mathrm{osc}}}\right)^2 P_{\mathrm{QVCO}}\right) \tag{7}$$

where S_{SSB} is single-side band phase noise in dBc/Hz at frequency offset Δf, f_{osc} is the oscillation frequency and P_{QVCO} is the total power consumption in milliwatts. Taking the tuning range into account, for the overall performance of the QVCO, FOM_T can also be adopted

$$\mathrm{FOM}_T = \mathrm{FOM} - 10\log\left(\frac{\mathrm{FTR}}{\Delta V_{\mathrm{tune}}}\right) \tag{8}$$

in which FTR and ΔV_{tune} are frequency tuning range and variation of tuning voltage, respectively.

As shown in Table II, the proposed QVCO has a much higher FOM, as well as wide tuning range and good phase accuracy.

To estimate the phase error, a Monte Carlo analysis with 3% standard deviation for all device mismatches including inductors, MIM capacitors and transistors dimensions and process variation is performed. Monte Carlo simulation results show an average phase error no more than 0.45° for the proposed QVCO.

Colpitts Multiphase VCO. Coupling of N identical LC-VCOs in a loop such that the $N-1$ core VCOs are coupled to each other in an "in-phase" manner, and the Nth core is coupled to the first one in an "anti-phase" manner [15] is a widely used technique for multiphase signals generation. Extending the same concept to the proposed structure, as shown in Fig. 6, the proposed coupling technique can be applied to several core Colpitts VCOs to generate multiphase signals. The proposed multiphase VCOs can generate multiphase signals with π/N phase differences ($N = 1, 2, 3, \ldots$ is the number of core VCOs).

As a typical case, a four-stage multiphase Colpitts VCO is implemented and simulated with circuit parameter values of Table I in a 0.18-μm RF-CMOS technology. The extracted simulation results show that the phase noise of the proposed four-phase VCO is -139 dBc/Hz

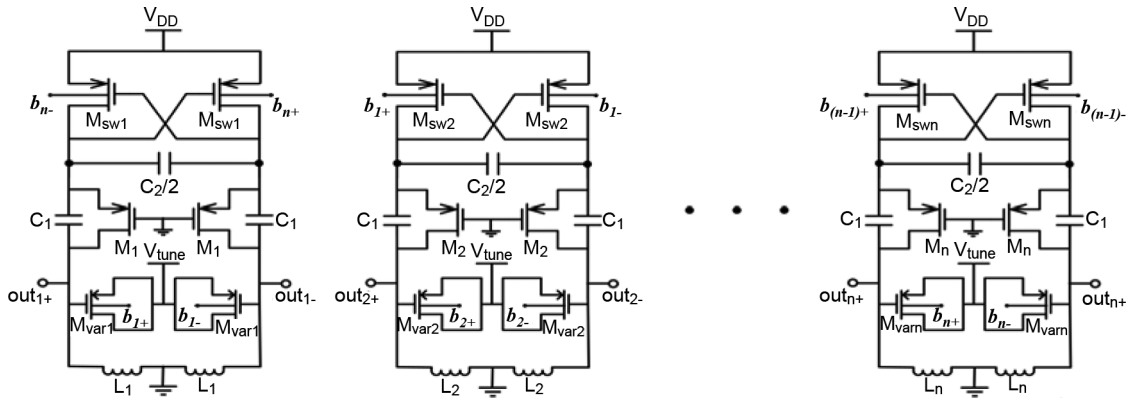

Fig. 6. Proposed multiphase VCO: $N-1$ core VCOs are coupled to each other in an in-phase manner and the Nth VCO is coupled to the first VCO in an anti-phase manner through the bulks of the core transistors.

at 3 MHz frequency offset from 5.25 GHz center frequency, while drawing 10.5 mA from a 1.8-V power supply, giving an $\mathrm{FOM} = -191.1$ dBc.

IV. Conclusion

Injection-locked quadrature oscillators are typically comprised of two distinct parts: two core VCOs and several coupling devices, in which each part contributes to the phase noise performance. To enhance the phase noise performance of the overall QVCO, the noise contribution of each part should be minimized. In this paper, conventional LC-VCOs are replaced with the noise-wise superior current-switching Colpitts VCOs. In addition, to reduce the noise sources and power dissipation due to the coupling circuitry, coupling devices were eliminated by utilizing the bulks of switching transistors and the bulks of the MOS varactors in the Colpitts core. An analysis of the operation of the proposed QVCO using a linearized model of the circuit is presented and shows agreement with simulation results. The proposed technique can also be used to couple N identical Colpitts VCOs for generation of multiphase signals.

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