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Power Factor Corrected Zeta Converter Based Improved Power Quality Switched Mode Power Supply

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***Abstract*—Multiple output Switched Mode Power Supplies (SMPSs) for personal computers (PCs) normally depict extremely bad power quality indices at the utility interface such as total harmonic distortion of the input current being more than 80%, power factor being lower than 0.5 and output voltage regulation being very poor. So, they violate the limits of harmonic emissions set by international power quality standards. In this paper, a nonisolated power factor corrected (PFC) converter is being proposed to be used at the front end to improve the power quality of an SMPS for a PC. The front end converter is able to reduce the 100 Hz ripple in its output that is being fed to the second stage isolated converter. The performance of the front-end Zeta converter is evaluated in three different operating conditions to select the best operating condition for the proposed SMPS system. The performance of the proposed SMPS is simulated and a laboratory prototype is developed to validate its performance. Test results are found to be in line with the simulated performance under varying input voltages and loading conditions and all the results demonstrate its enhanced performance.**

***Index Terms* --Power factor corrected Zeta converter, unity power factor, power quality, SMPS, multiple outputs**

I. Introduction

In the present era, personal computers (PCs) have become a part of our day to day activities from business to education to infotainment. Switched Mode Power Supply (SMPS) is an integral part of the computer that converts ac to multiple numbers of suitable dc voltages to impart power to different parts of the PC. It contains a diode bridge rectifier (DBR) with a capacitor filter followed by an isolated dc-dc converter to achieve multiple dc output voltages of different ratings. The uncontrolled charging and discharging of the capacitor result in a highly distorted, high crest factor, periodically dense input current at the single phase ac mains; this violates the limits of international power quality (PQ) standards such as IEC 61000-3-2 [1-2]. Further, the neutral current in the distribution system increases if these PCs are used in large numbers which creates serious problems like overloading the neutral conductor, noise, de-rating of the transformer, voltage distortion etc. [3-5].

To end these problems, improved PQ SMPSs that are capable of drawing a sinusoidal input current at unity power factor (UPF) and yielding stiffly regulated output voltages, are extensively being researched. Employing various power factor corrected (PFC) single-stage and two stage converters effect a perceivable PQ improvement in these SMPSs [6-10]. PQ improvement is visible in the form of low total harmonic distortion (THD) in the ac mains current and power factor being close to unity at the point of common coupling (PCC). This is achieved even under varying loads and supply voltage conditions. In a single-stage SMPS, ac supply is connected to a DBR whose output is processed by a multi-output PFC isolated dc-dc converter for obtaining dc voltages. The reliability of this single-stage SMPS is good; however, the output capacitors used are of very high value to reduce the 100 Hz ripple content. So, the rating of any single-stage SMPS is limited to about 200 W to avoid prohibitively high capacitance value.

For medium power ratings, two stage SMPS is a commonly accepted solution in the SMPS market for PCs. The first stage is meant for improving the power quality at the PCC and for providing regulated dc output voltage to the isolated (second) stage. The selection of operating mode of the front end converter may be in Discontinuous Conduction Mode (DCM) if the cost is a major consideration; if not, Continuous Conduction Mode (CCM) is adopted that reduces device stresses, despite the fact that CCM uses two voltage and one current sensors which naturally makes it costlier. Therefore, a DCM operation of the front end PFC converter is preferred in PCs where only one voltage sensor is needed for sensing and control.

A boost converter is a common choice as a PFC in various industrial applications. However, it cannot be used if a wide range of ac mains voltage is to be taken care of [11]. Similarly, due to limited output voltage range buck converters are not preferred for computer power supply [12]. Non-isolated buck-boost PFC converter configurations are the best suited for maintaining a constant dc output voltage irrespective of wide variations in ac supply voltages. Different buck-boost converters configurations and their application to SMPS are reported in the literature [13-19]. A conventional buck-boost converter has a low component count. However, the output

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current is pulsating in nature which increases the ripple in voltage. The buck-boost Cuk converter is not preferred due to the polarity of the output being reversed which gives rise to various design issues. SEPIC also depicts a pulsating output current. As the output stage of the power supply is very sensitive, this pulsating current is not desirable. The flyback converter suffers from leakage inductance problem which imposes a limit on its rating. To eliminate these issues, a Zeta PFC converter is employed as a PFC converter in many research papers. It provides a continuous output current with a low ripple output voltage along with a high level performance which is highly recommendable for PCs. The dynamic modeling of the Zeta converter is carried out using state space averaging technique in [20-24]. The suppression of lower order harmonic content leads to reduction in EMI of a PFC ac-dc converter operating in DCM as discussed in [25]. An isolated converter is required at the output for yielding multiple dc output voltages in an SMPS for PCs. An isolated half-bridge dc-dc converter is preferred here because of excellent core utilization and less device stress [26-29].

This paper presents power quality improvement in a multiple output SMPS that yields regulated dc output voltages irrespective of line and load variations. A Zeta PFC converter is still unexplored for the development of computer SMPSs that are capable of drawing a purely sinusoidal current with unity PF, offering low rippled output which is the prime requirement of PCs. In this work, three different operating modes of the Zeta converter have been analyzed and compared to select the best operating mode for a computer power supply application [23-24]. The proposed SMPS is designed, modeled and simulated in MATLAB/Simulink platform [30] to validate the design. Then, an experimental prototype is built in the laboratory and tests are conducted on it. The recorded test results on the developed prototype are in line with the simulation results confirming the validity of the design.

II. Proposed PFC Zeta Converter Based SMPS Configuration

Fig. 1 shows the system configuration of a PFC Zeta converter based multi-output SMPS topology. At the input, a DBR with filter is connected to a nonisolated Zeta converter. It consists of two inductors L_{z1} and L_{z2}, one intermediate capacitor C_1, one high frequency switch S and one diode D. This PFC converter regulates the output dc voltage and draws a sinusoidal current from the ac mains at unity PF. Three different DCM conditions (i.e. input inductor DCM, intermediate capacitor DCM and output inductor DCM) are considered here to choose the best operating condition of the front end PFC converter. In the DCM operation, the current becomes zero either in the input inductor or output inductor, or the voltage across the intermediate capacitor becomes zero for some duration in one switching cycle. The output dc voltage is regulated using a Proportional-Integral (PI) voltage controller. The regulated output dc voltage is connected to an isolated converter for achieving multiple dc voltages at the output. The isolated converter consists of two equal valued input capacitors, two switches, one high frequency transformer (HFT) and filters. The filters are used in each output winding to reduce the output voltage and current ripples. Only one of the output voltages is directly sensed and the other output voltages are controlled by the duty cycle of the isolated converter. The winding that is selected for control action is of the largest power rating among all the outputs. Further, to reduce the component stresses, the isolated converter is designed in CCM. Another voltage PI controller is used here to regulate the output voltage. The performance of the proposed PFC Zeta converter based SMPS is demonstrated for a wide variation in the input voltages from 170V to 260V and loads with the input power quality indices recorded for each of these operating conditions.

III. Operating Principle of the Proposed SMPS

The operation of the proposed SMPS is studied to analyze its behavior in one switching cycle. Three different conditions (input inductor in DCM, intermediate capacitor in DCM,

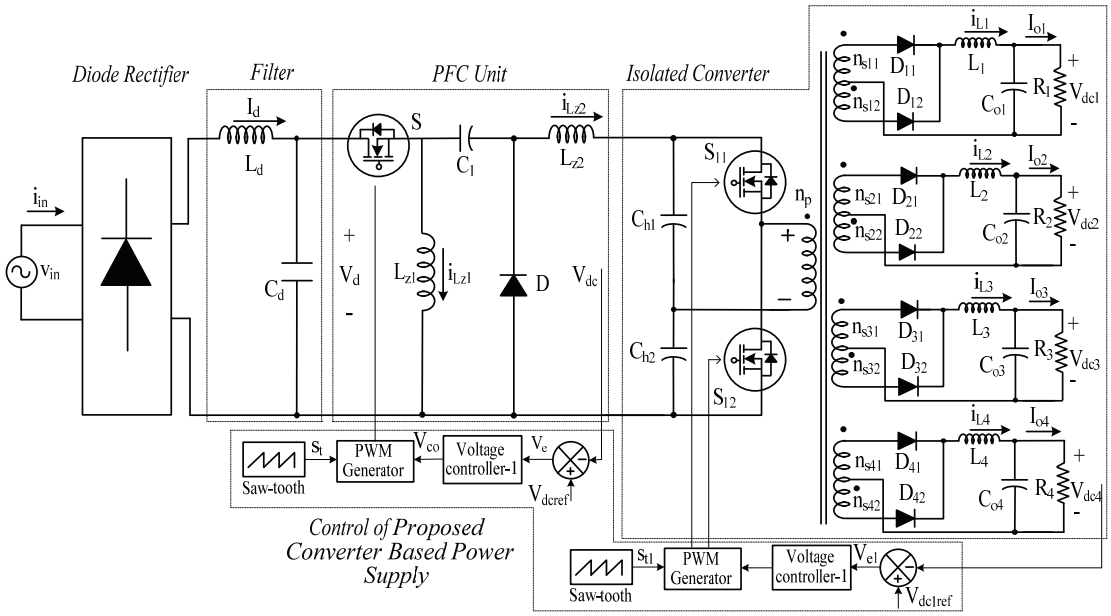

Fig.1. PFC Zeta converter based SMPS for PCs

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output inductor in DCM) have been considered for the PFC Zeta converter to select the best operating condition.

A. PFC Converter Operation When Input Inductor is in DCM

Fig. 2 shows the operation of a PFC Zeta converter when the input inductor is in DCM. The current in the input inductor remains zero for some time in one switching cycle while the current in the output inductor and voltage across the intermediate capacitor remain non-zero.

1) Mode I: When the PFC switch S turns on, the current in the input inductor L_{z1} and output inductor L_{z2} start increasing and the voltage across the capacitor starts decreasing.

2) Mode II: When S is turned off, diode D starts conducting as shown in Fig. 2(b). The stored energy in L_{z1} starts decreasing and continues until the current i_{Lz2} equals the negative of the current i_{Lz1}. The voltage across the intermediate capacitor C_1 starts increasing.

3) Mode III: Both switch S and diode D are off in this period of one switching cycle as shown in Fig. 2(c). This state lasts until the start of the next PWM cycle. The input inductor current i_{Lz1} remains zero ensuring the DCM condition.

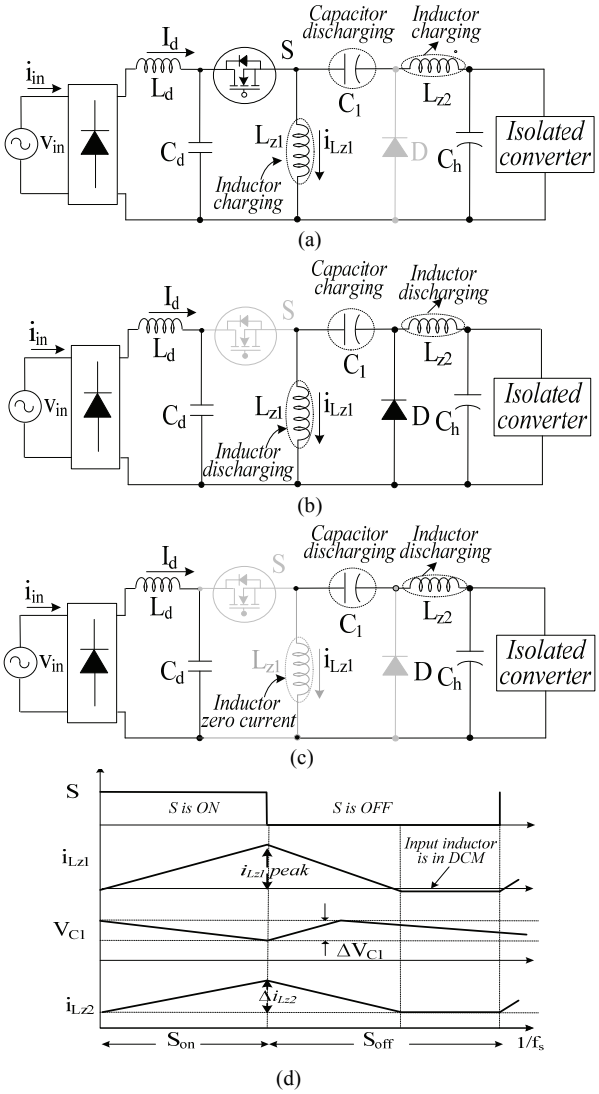

Fig. 2. Operating modes of the PFC Zeta converter in one switching cycle when L_{z1} is in DCM, (a) When input inductor is charging, (b) When input inductor is discharging, (c) when input inductor is in zero current mode, (d) Waveforms of various components in one switching cycle

B. PFC Converter with Intermediate Capacitor in DCM

The operation of a PFC Zeta converter, when the intermediate capacitor is operating in DCM, is shown in Fig. 3. The three switching states are described as follows:

1) Mode I: When switch S turns on, the currents in inductors L_{z1} and L_{z2} are increasing while the intermediate capacitor discharges through the output inductor L_{z2}; the voltage across the output capacitor increases.

2) Mode II: In this mode, switch S is in conduction state but the intermediate capacitor C_1 is completely discharged and the voltage across C_1 becomes zero. In this condition, output inductor L_{z2} continues to supply energy to the output capacitor.

3) Mode III: Switch S now turns off, input inductor L_{z1} is discharging through the intermediate capacitor. The output inductor L_{z2} is discharging through the isolated converter while maintaining continuous conduction.

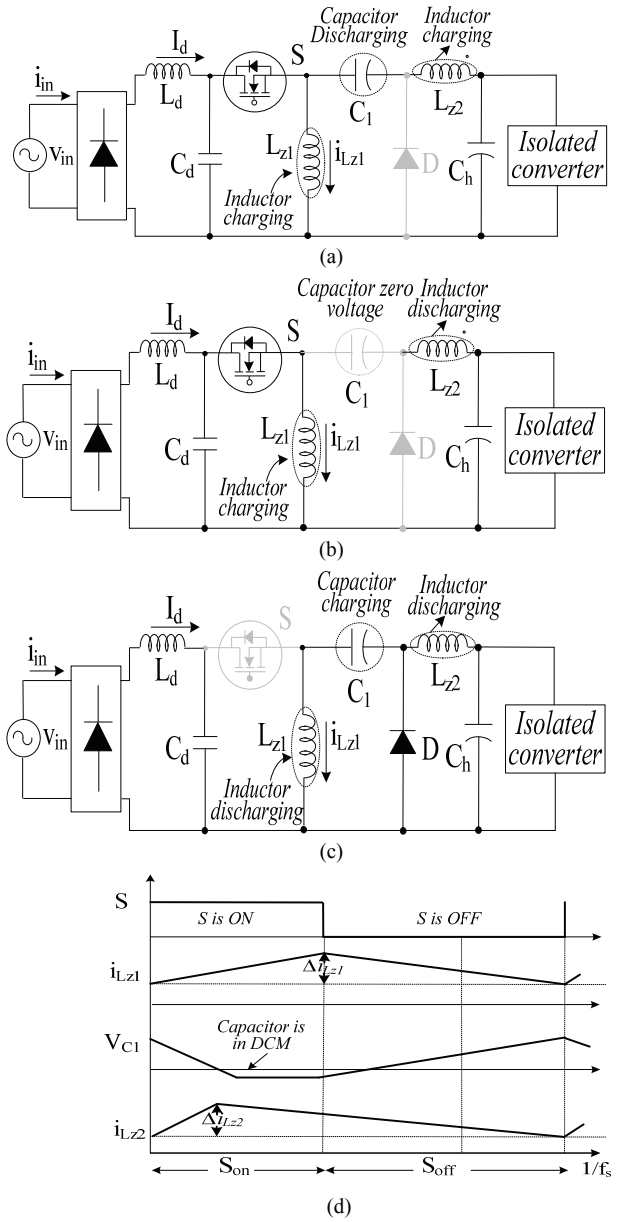

Fig. 3. Operating modes of the PFC Zeta converter in one switching cycle when C_1 is in DCM (a) When capacitor is discharging, (b) When capacitor is in zero voltage mode, (c) When capacitor is charging, (d) Waveforms of various components in one switching cycle

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C. PFC Converter with Output Inductor in DCM

The DCM operation of the output inductor in one switching cycle is shown in Fig. 4. The output inductor is designed in DCM and therefore, the current in the output inductor remains zero for a certain time period in one switching cycle. The different modes of conduction in one switching cycle are described as follows.

1) Mode I: The PFC switch S turns on; the input voltage supplies energy to inductor L_{z1}. The intermediate capacitor discharges through the output inductor L_{z2}. The currents in L_{z1} and the output inductor increase linearly.

2) Mode II: The switch S turns off and diode D turns on as shown in Fig. 4(b). The stored energy in L_{z1} is transferred to the capacitor C_1; the output inductor energy is fed to the isolated converter. This stage continues until the current i_{Lz1} equals the negative of the current i_{Lz2}.

3) Mode III: The switch and diode both are off in this duration of one switching cycle as shown in Fig. 4(c). This state lasts until the start of the next PWM cycle. The output inductor current remains zero in the remaining time ensuring the DCM condition.

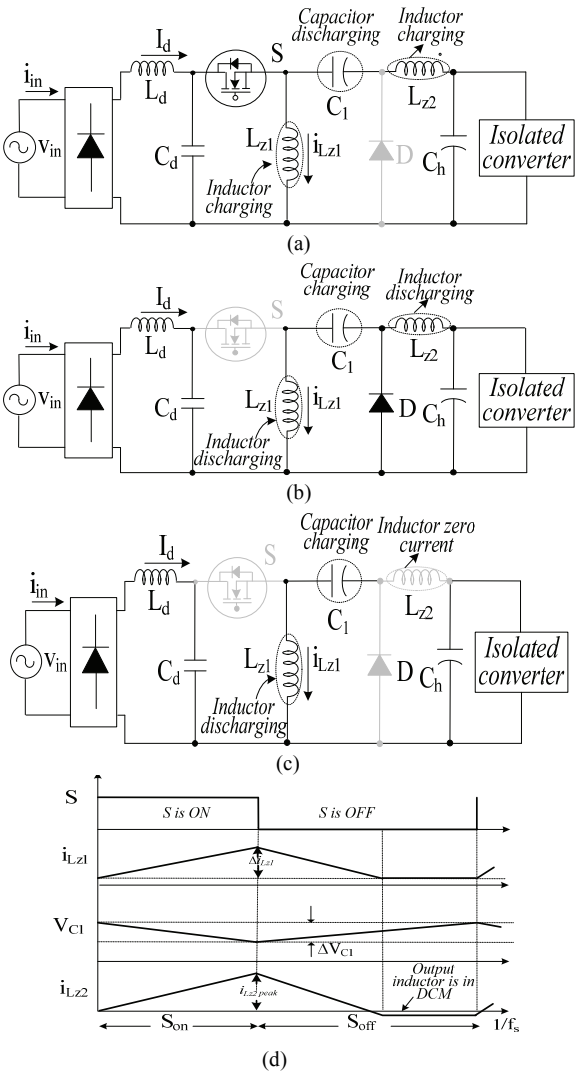

Fig.4. Operating modes of the PFC Zeta converter in one switching cycle when L_{z2} is in DCM (a) When output inductor is charging, (b) When output inductor is discharging, (c) when output inductor is in zero current mode, (d) Waveforms of various components in one switching cycle

D. Isolated Converter

The operation of the isolated half-bridge converter working in CCM is described in two states during one half of the switching cycle (Fig. 5) where the upper switch is involved. In the second half of one switching cycle, the same procedure repeats with the involvement of the lower switch.

1) Inductor Charging

The output voltage of the PFC Zeta converter is connected to one end of the primary winding of the HFT through switch S_{11}. Diodes D_1, D_3, D_5, D_7 start conducting. So, the output currents i_{Lo1}, i_{Lo2}, i_{Lo3} and i_{Lo4} in inductors increase. When the inductor current reaches its maximum value, S_{11} is turned off.

2) Inductor Discharging

The output inductor current in each secondary winding freewheels through corresponding diodes (D_1-D_8). The current in each winding cancels the flux until the voltages across all windings are reduced to zero.

The same inductor charging and discharging take place in the next half of the switching cycle when the lower switch turns on and then turned off subsequently.

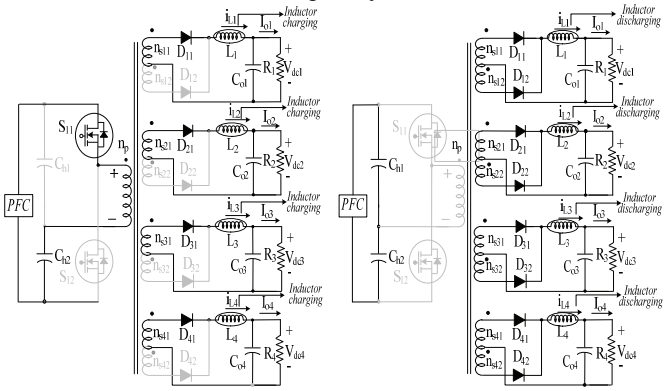

Fig.5. Operating modes of the isolated converter in one half of the switching cycle

IV. Design of the Proposed PFC Zeta Converter Based SMPS

The design of PFC Zeta converter based SMPS is carried out in this section. The design is based on the change in the inductor current during the switch on and off period. The diodes and switches are considered ideal. The switching frequency considered is high as compared to the line frequency; so, average magnitudes (of currents and voltages) within a PWM period are considered for analysis.

The relation between output voltage, V_{dc} and input voltage V_d of the Zeta buck-boost converter is expressed as,

$$\frac{V_{dc}}{V_{in}(t)} = \frac{D}{1-D} \quad (1)$$

Therefore, the instantaneous value of duty ratio, D(t) is expressed as,

$$D(t) = \frac{V_{dc}}{V_{in}(t)+V_{dc}} \quad (2)$$

A. Input Inductor Selection

The critical inductance value of the input inductor is,

$$L_{z1min} = \frac{D(t)TV_{in}(t)}{2I_{in}} = \frac{R_{in}D(t)T}{2} = \frac{V_d^2 D(t)T}{2P_{in}} = \frac{V_d^2 T}{2P_{in}}\left[\frac{V_{dc}}{V_{in}(t)+V_{dc}}\right] \quad (3)$$

$$=\frac{(153.1V)^2*50\mu S}{2*350W}\left[\frac{300V}{(1.414*170V)+300V}\right]=0.92mH$$

where V_d is the uncontrolled dc voltage, D is the duty ratio, T is the total switching time in one switching cycle (here, 50μs). The critical value of input inductor L_{z1} is proportional to the rms value of supply voltage. Therefore, the worst case design occurs for the minimum value of supply voltage of 170V. The minimum input inductor value from eqn. (1) is 0.92 mH. The selected value of inductor L_{z1} is 0.2 mH for maintaining it in DCM under all operating condition.

To design the input inductor in CCM, its minimum value is expressed as,

$$L_{z1min}=\frac{D(t)TV_{in}(t)}{\Delta i_{in}(t)}=\frac{V_{in}(t)T}{\Delta i_{in}(t)}\left[\frac{V_{dc}}{V_{in}(t)+V_{dc}}\right] \quad (4)$$

$$=\frac{1.414*170V*50\mu S}{0.50*2.05A*1.414}\left[\frac{300V}{1.414*170V+300V}\right]=4.6mH$$

Hence, a 5mH is selected for CCM operation of the input inductor.

B. Output Inductor Selection

The critical value of output inductor is estimated as,

$$L_{z2min}=\frac{(1-D(t))TV_{dc}}{2I_{dc}(t)}=\frac{V_{dc}DT}{2I_{in}(t)}=\frac{R_{in}V_{dc}D(t)T}{2V_{in}(t)}=\frac{V_d^2TV_{dc}}{2V_{in}(t)P_{in}}\left[\frac{V_{dc}}{V_{in}(t)+V_{dc}}\right] \quad (5)$$

$$=\frac{(153.1V)^2*50\mu S*300V}{2*350W*1.414*170V}\left[\frac{300V}{1.414*170V+300V}\right]=1.15mH$$

The maximum current ripple in this inductor occurs at the maximum power and for minimum value of supply voltage (170V). So, the minimum inductance value for operating the output inductor in DCM is estimated as 0.7mH.

Similarly, L_{z2} while operating in CCM is expressed as,

$$L_{z2min}=\frac{(1-D(t))TV_{dc}}{\Delta I_o}=\frac{V_{dc}DT}{\Delta I_{in}(t)}=\frac{V_{dc}T}{\Delta I_{in}(t)}\left[\frac{V_{dc}}{V_{in}(t)+V_{dc}}\right] \quad (6)$$

$$=\frac{300V*50\mu S}{0.5*2.05A*1.414}\left[\frac{300V}{170V*1.414+300V}\right]=5.75mH$$

The selected value of inductor L_{z2} is 6mH for maintaining it in CCM.

C. Intermediate Capacitor Selection

The capacitor is used to transfer energy from the input to the output in a controlled manner. The intermediate capacitor C_1 experiences two conflicting constraints, namely, it should have nearly a constant value of voltage within one PWM cycle and also follows the input voltage profile in line frequency period. The value of intermediate energy transfer capacitor is calculated from a given value of voltage ripple as,

$$C_1=\frac{D(t)TV_{dc}}{2V_{C1}R_{dc}}=\frac{TV_{dc}}{2\{V_{dc}+V_{in}(t)\}(V_{dc}^2/P_{in})}\left[\frac{V_{dc}}{V_{dc}+V_{in}(t)}\right]=\frac{TP_{in}}{2(V_{dc}+V_{in}(t))^2} \quad (7)$$

$$=\frac{50\mu S*350W}{2(300V+270V*1.414)^2}=18.8nF$$

For DCM operation, the capacitance value is selected as 14nF.

$$C_1=\frac{D(t)TV_{dc}}{2\Delta V_{C1}R_{dc}}=\frac{TV_{dc}}{2\{\Delta(V_{dc}+V_{in}(t))\}(V_{dc}^2/P_{in})}\left[\frac{V_{dc}}{V_{dc}+V_{in}(t)}\right]=\frac{TP_{in}}{2\{\Delta(V_{dc}+V_{in}(t))\}(V_{dc}+V_{in}(t)} \quad (8)$$

$$=\frac{50\mu S*350W}{2\{0.3(300V+270V*1.414)\}(300V+270V*1.414)}=0.0628\mu F$$

where, Δ is the permitted ripple in the intermediate capacitor voltage. The selected value of intermediate capacitor is of the order of 0.066μF for maintaining it in CCM under all operating conditions.

D. Output Capacitor Selection

The input capacitor(s) of the isolated converter also works as the output capacitor of the Zeta converter. It is selected such that it eliminates the second order harmonic voltage introduced due to the single phase ac mains. The output capacitor value is selected as,

$$C_h=\frac{I_{dc}}{2\omega\Delta V_{dc}} \quad (9)$$

The estimated output capacitors are calculated as 400 μF for a 9V ripple. The selected value of output capacitors C_{h1}=C_{h2} are taken as 330 μF in hardware.

E. Filter Design

The input filter design is very important for maintaining low harmonic distortion at the input ac mains [31]. The maximum filter capacitance is expressed as,

$$C_{max}=\frac{I_p\tan\theta}{2*\pi*f*V_p} \quad (10)$$

where V_p and I_p are the peak input voltage and current and θ is considered 1° for maintaining high PF. The maximum capacitance C_{max} is estimated as 0.4 μF and the selected value C_d in hardware is 330nF.

The filter inductor to maintain low ripple is calculated as,

$$L_d=\frac{1}{4*\pi^2*f_c^2*C_d} \quad (11)$$

where f_c is the cut-off frequency which is selected such that it is more than the fundamental frequency (f=50Hz) and less than switching frequency f_s(20 kHz). Therefore it is taken as 2 kHz here. L_d from the above equation is calculated as 3.1mH and the selected value in hardware is 3mH. The selected component values are tabulated in Table I.

TABLE-I
SELECTED VALUES FOR THE PFC CONVERTER FOR THE POWER SUPPLY

Component	Calculated	Selected	Experimental
Input inductor L_{z1}	4.6mH	5mH	5mH
Input inductor L_{z2}	1.15mH	0.7mH	0.7mH
Capacitor C_1	0.062μF	66nF	66nF
Filter capacitor C_d	400nF	330nF	330nF
Filter inductor L_d	3.1mH	3mH	3mH
Capacitor C_{h1} and C_{h2}	630μF	660μF	660μF

V. CONTROL OF THE PROPOSED PC SMPS

Two independent controllers are used to control the dc output voltages of the PFC converter and the isolated converter [21, 23]. The front end converter is controlled using voltage follower approach while the isolated converter utilizes average current control.

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A. Control of PFC converter

The control of the front end PFC converter generates pulses according to the output voltage error, which is the voltage difference between the desired voltage and sensed voltage. The voltage error signal (V_e) at n^{th} instant is,

$$V_e(n) = V_{dcref}(n)-V_{dc}(n) \quad (12)$$

V_e is fed to the proportional–integral (PI) controller to generate a controlled output voltage (V_{co}).

$$V_{co}(n)=V_{co}(n-1)+k_p\{V_e(n)-V_e(n-1)\}+k_iV_e(n) \quad (13)$$

where k_p and k_i are the proportional and integral gains of the PI controller.

The output of the PI controller is compared with a high frequency saw-tooth signal (S_t) to generate the PWM pulses.

If $S_t<V_{co}$, then S=on, else S=off

where, S represents the switching signals for the PFC converter device. If the output voltage varies, the control output voltage V_{co} changes to vary the duty cycle. Hence, the width of PWM pulses changes accordingly to maintain the dc output voltage as a constant.

B. Control of Isolated Converter

To control the multiple dc output voltages of the isolated converter, average current control scheme is used. Only one winding's output voltage which is having the highest power rating is controlled. The other windings' output voltages are controlled by the duty cycle of the converter as a common core is used for all secondary windings. The responses of the other windings are slow as compared to the output whose voltage is sensed. For control, output voltage V_{dc1} is sensed and compared with the corresponding reference voltage to produce voltage error which is the input to the PI controller. The output of this PI controller is compared with a saw-tooth wave to generate the switching pulses for both the switches S_1 and S_2. Both the switches are switched on and off alternately in each half cycle of one PWM period with sufficient dead time to avoid shoot-through. The width of the pulses varies according to the voltage error. Thus, the control of isolated converter is able to take care of the impact of other output voltage variations (due to load changes in these outputs) by modifying the duty ratio. If any winding undergoes a load change, the duty ratio changes according to the impact felt on the sensed output to maintain voltage regulation on all the outputs.

V1. Performance Evaluation

The performance of the proposed Zeta converter based SMPS is studied through simulation results to select the best mode of operation. The design specifications for the power supply are given in Table II. The power supply is modeled in MATLAB/Simulink using discrete sampling mode. The performance of the power supply is analyzed under three operating conditions of DCM.

TABLE-II
DESIGN SPECIFICATIONS OF THE ZETA CONVERTER BASED SMPS

Specifications	Values
Input voltage	220V(ac)
Output voltage/Output current	12V/12.5A
	5V/23A
	3.3V/16A
	-12V/0.8A
Switching frequency of isolated converter	60 kHz

1) When L_{z1} is operating in DCM: Fig. 6(a) shows the waveforms of v_{in}, i_{in}, i_{Lz1}, i_{Lz2}, v_{C1}, v_S, i_S when the input inductor is operating in DCM. The current through the output inductor i_{Lz2} and voltage of the intermediate capacitor V_{C1} remain in continuous conduction while the current in input inductor is in DCM. The peak voltage and current stresses of the PFC switch are observed to be 630V and 28A respectively in this condition. The input current THD is 4.11% at full load as shown in Fig. 6(b).

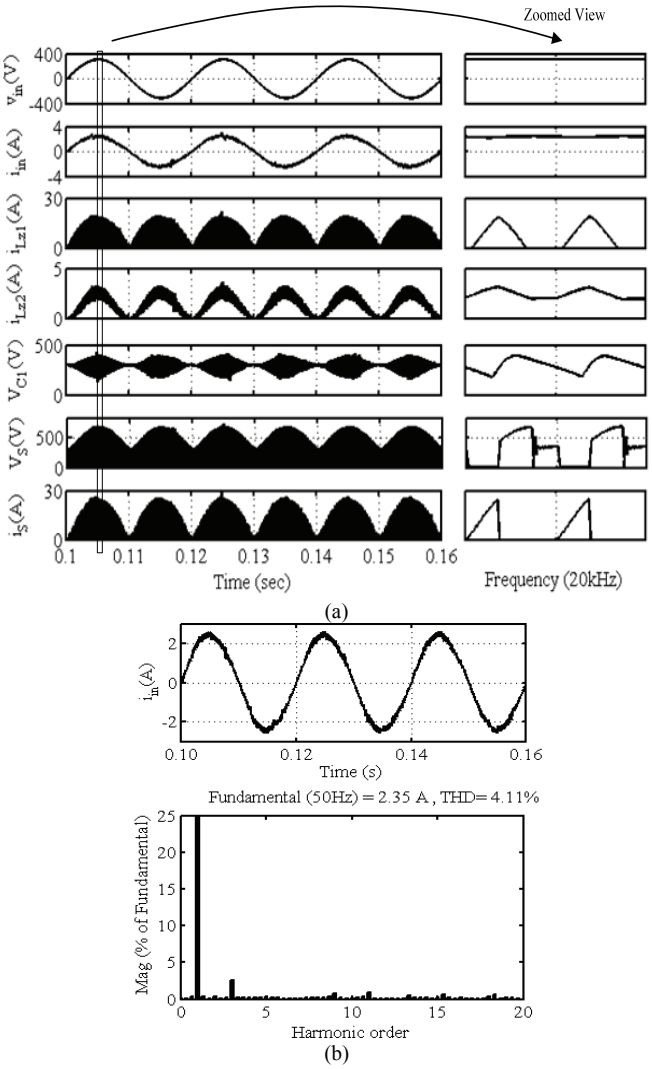

Fig.6. Waveforms of PFC converter when L_{z1} is operating in DCM (a) Waveforms of v_{in}, i_{in}, i_{Lz1}, i_{Lz2}, V_{C1}, V_S, I_S at 220V, (b) Input current and its harmonic spectrum

2) When C_1 is operating in DCM: The waveforms of various electrical quantities of the PFC Zeta converter operating in discontinuous voltage of the intermediate capacitor are shown in Fig. 7(a). It is clearly seen that V_{C1} remains discontinuous for some time in one switching cycle while the currents in input and output inductors (i_{Lz1} and i_{Lz2}) remain continuous. The peak current stress of the switch is observed of the order of 12.3A which is much lower than the previous case. However, the peak voltage stress is 1980 V at rated condition which is very high and makes this configuration difficult to be realized in practice. The input current THD in this mode is 4.30% (Fig. 7(b)).

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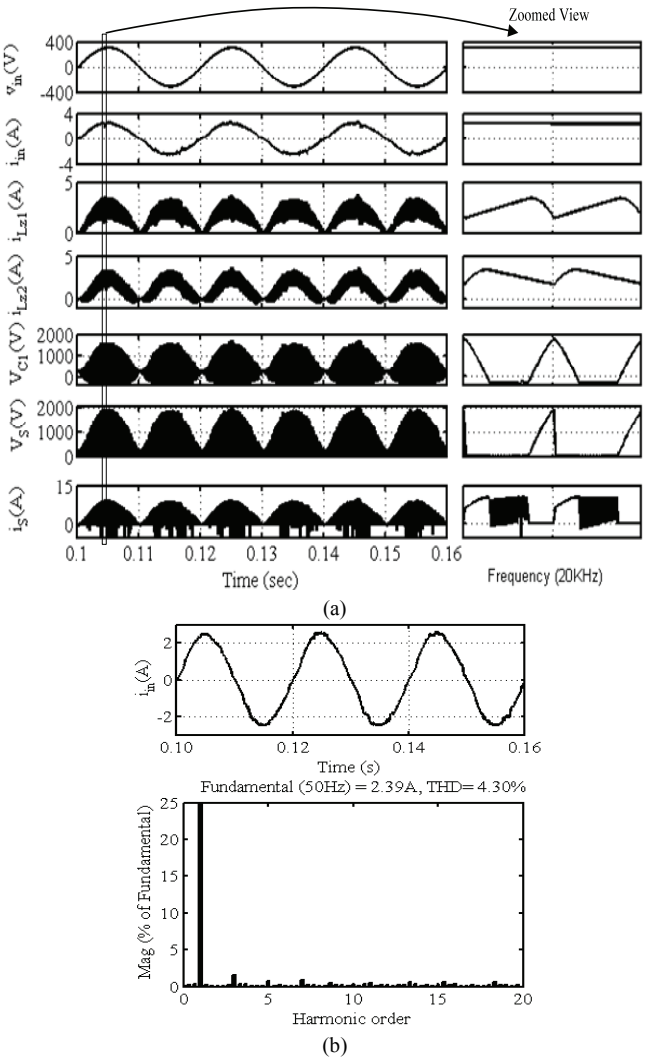


Fig.7. Waveforms of PFC converter when C_1 is operating in DCM (a) Waveforms of v_{in}, i_{in}, i_{Lz1}, i_{Lz2}, V_{C1}, V_S, I_S at 220V, (b) Input current and its harmonic spectrum

3) When L_{z2} is operating in DCM: The output inductor is operating in DCM and corresponding current touches zero in each PWM cycle; the waveforms are shown in Fig. 8(a). The peak voltage and current stresses of 600V and 24A are observed for the switch, which is quite acceptable for a power rating of 350W. The THD of input current observed under full load is 3.07% as shown in Fig. 8(b).

Thus, the observed performance of the proposed SMPS in all three operating conditions is well within the international power quality limits and hence the designs are validated. The voltage stress of the switch is unacceptably high when the intermediate capacitor operates in DCM. The voltage stresses for the L_{z1} and L_{z2} in DCM are of the order of 620V which is quite acceptable. However, peak current stress is slightly lower when L_{z2} is operating DCM which makes it suitable for the PC application. Moreover, the current in input inductor L_{z1} and voltage across intermediate capacitor V_{C1} are maintained in CCM which verifies the design. The voltage stress of the intermediate capacitor is observed to be 340V which is quite satisfactory. Based on this analysis, a hardware prototype of the Zeta converter based SMPS with L_{z2} in DCM is developed and discussed in the following sections.

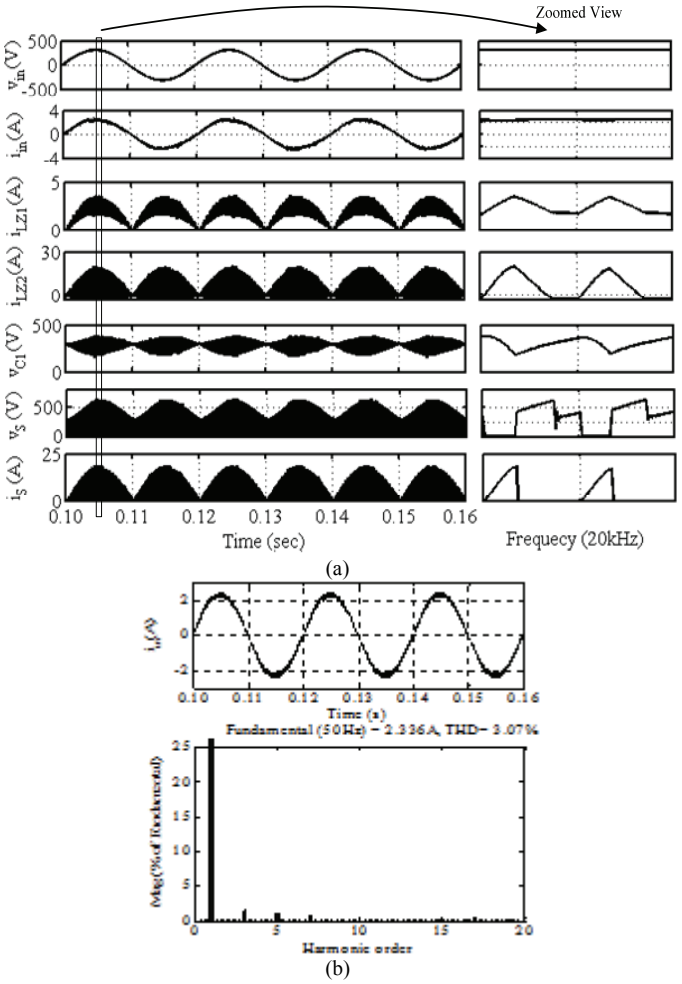


Fig.8. Waveforms of PFC converter when L_{z2} is operating in DCM (a) Waveforms of v_{in}, i_{in}, i_{Lz1}, i_{Lz2}, V_{C1}, V_S, I_S at 220V, (b) Input current and its harmonic spectrum at full load

VII. Hardware Verification

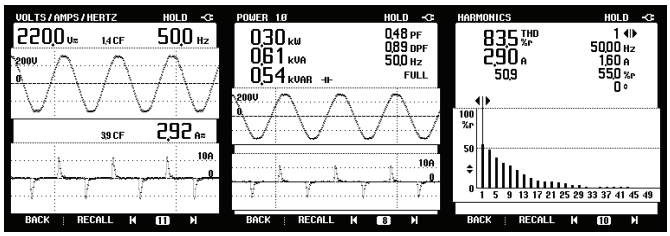
The design and simulated performances of the proposed SMPS given in the previous section are validated through developed hardware when the front end Zeta converter is operating with L_{z2} in DCM. The output voltage is controlled and regulated by means of a Digital Signal Processor (DSP). A 20 kHz switching frequency is used to gate the switch of the Zeta converter for effective control and reduction in component size. Test results are recorded by using a digital storage oscilloscope and single phase power analyzer. The experimental performance of the proposed Zeta PFC converter based SMPS is described in this section.

A. Comparison with Conventional SMPS

Recorded test results for a conventional SMPS at rated voltage are shown in Fig. 9. The THD of input current is 83.5% and the PF is as low as 0.48 (Figs.9(c) and 9(b)). The SMPS draws periodically dense, peaky, harmonic rich input current. Thus, the performance of conventional SMPS grossly violates the international PQ standards set by IEEE and IEC. To maintain PQ within the limits of international standards and to regulate the dc voltage effectively, it is recommended that a PFC based front end converter may be used for the SMPS that draws sinusoidal input current with unity PF.

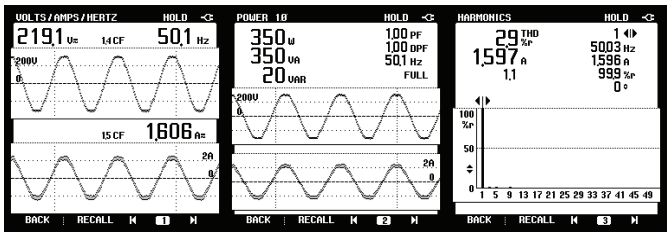
B. Performance of Proposed SMPS under Varying Input Voltages

Fig. 10 shows the recorded test results of the proposed SMPS under rated load and input voltage conditions which show that the PF is unity with THD of input current being 2.9%. Fig. 11(a) shows the input voltage, input current and the output voltage of the Zeta converter along with the output current. The output voltage is maintained constant due to closed loop control. The output voltages of the second stage converter i.e., +5V output and +3.3 V output along with their respective load currents are shown in Figs. 11(b) and 11(c). Both the voltages are regulated stiffly to the specified values. Fig. 11(d) shows the test results of the input inductor current which is maintained in CCM while the output inductor current touches zero in each PWM cycle maintaining DCM as shown in Fig. 11(e) and the enlarged view is shown in Fig. 11(f). The capacitor voltage, input voltage and current are shown in Fig. 11(g). These recorded waveforms conform to the ones obtained by simulation hence validate the design and simulated results of the proposed SMPS. The maximum voltage and current of the switch are shown in Fig. 11(h) which shows that the voltage stress is 580V which is acceptable for a 220V input voltage. Test results of the proposed power supply during wide input voltage variations are shown in Figs. 12 and 13. The THD of the input current at 170V and 260V are respectively 2.3% and 3.5% and PF is unity as shown in Table-III falling within the IEEE-519 standard limit.



(a) (b) (c)

Fig. 9. Performance of the conventional SMPS (a) Input voltage and input current of the conventional SMPS for PCs, (b) Input power and PF, (c) Input current harmonic spectrum



(a) (b) (c)

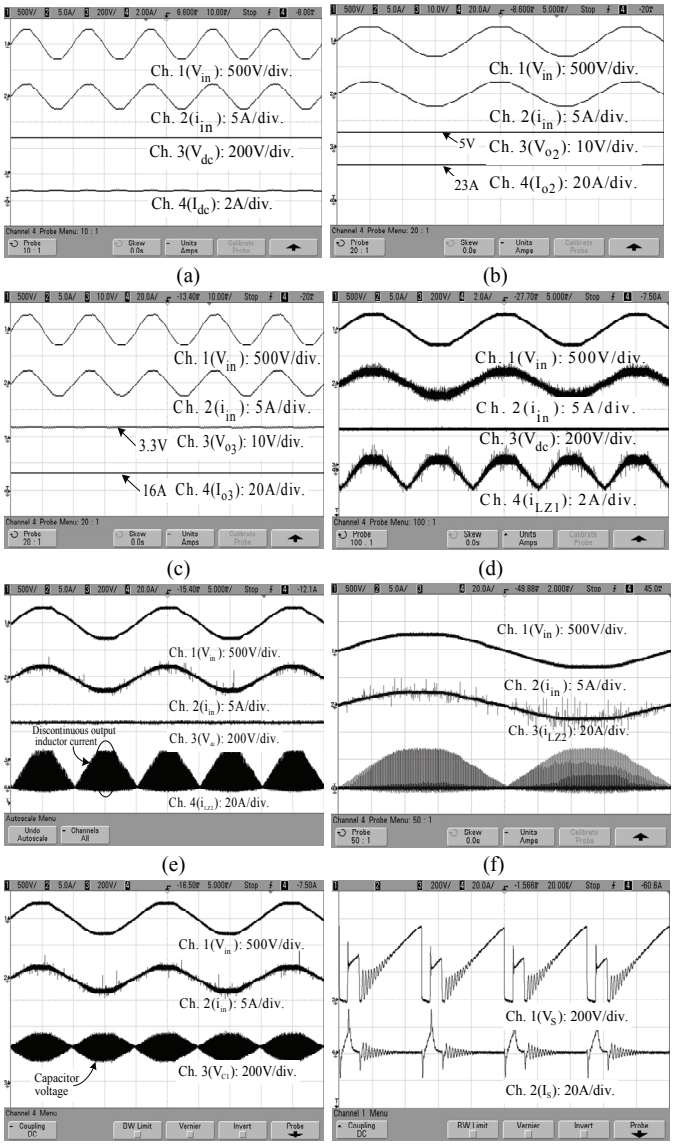
Fig. 10. Performance of the proposed SMPS (a) Input voltage/current at rated voltage, (b) Input power and PF, (c) Input current harmonic spectrum

TABLE-III
SMPS PARAMETERS AT VARIOUS INPUT VOLTAGES

Input voltage	Input Current	i_{THD}(%)	DPF	PF
170V	2.055	2.30	1	1
220V	1.606	2.9	1	1
260V	1.36	3.5	1	1

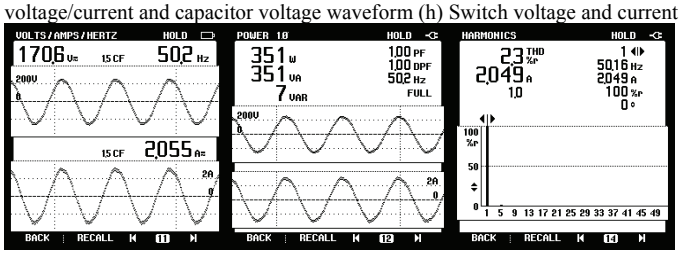
C. Performance under Light Load

Fig. 14 shows the performance of the PFC Zeta converter based power supply at light load (25% of rated load). The input current is reduced and it is maintained sinusoidal with unity PF. The THD of ac mains current at light load is observed as 4.5% as shown in Fig. 14(c) which adheres to the limit set by IEC standard [1]. Thus, a satisfactory performance with acceptable input current THD is obtained at the ac mains for varying input voltages and loads.



(a) (b) (c) (d) (e) (f) (g) (h)

Fig.11. Test results of the proposed power supply (a) AC mains voltage/ current and Zeta converter output voltage/current, (b) AC mains voltage/ current and +5V output voltage/current, (c) AC mains voltage/ current and +3.3V output/current, (d) AC mains voltage/current, output voltage and input inductor current, (e) AC mains voltage/current, output voltage and output inductor current, (f) Enlarged view of output inductor current (g) Input voltage/current and capacitor voltage waveform (h) Switch voltage and current



(a) (b) (c)

Fig.12. Performance of the proposed SMPS at 170V (a) AC mains voltage/current, (b) Input power and PF, (c) Input current harmonic spectrum

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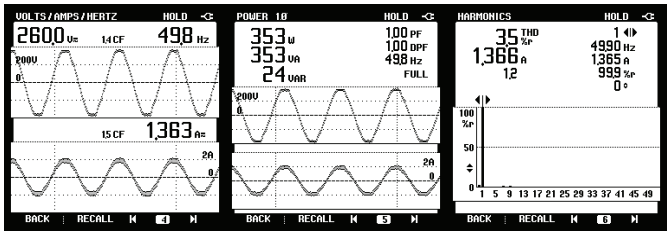
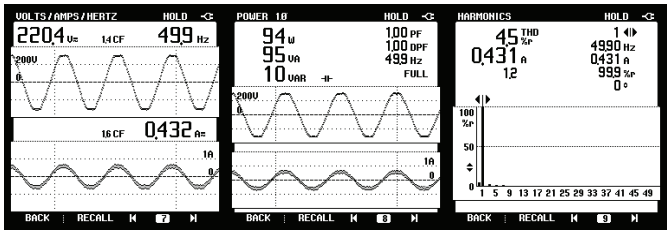


(a) (b) (c)

Fig.13. Performance of the proposed SMPS at 260V (a) AC mains voltage/current, (b) Input power and PF, (c) Input current harmonic spectrum



(a) (b) (c)

Fig.14. Performance of the proposed SMPS at light load (a) AC mains voltage/current, (b) Input power and PF, (c) Input current harmonic spectrum

Fig. 15 shows the efficiency of the conventional and the proposed SMPS at various loading conditions and input voltages. As the loading decreases, the efficiencies of the conventional and the proposed system also decrease. The efficiency of the SMPS system at full load is 88.8%. Although the efficiency of the proposed SMPS is lower than the conventional SMPS, the conventional SMPS is not recommended because of its high harmonic distortion, low PF and poor voltage regulation as shown in Fig. 9 violating the international PQ standard limits. It is observed that the proposed PFC based SMPS has a remarkably improved performance as compared to the conventional SMPS.

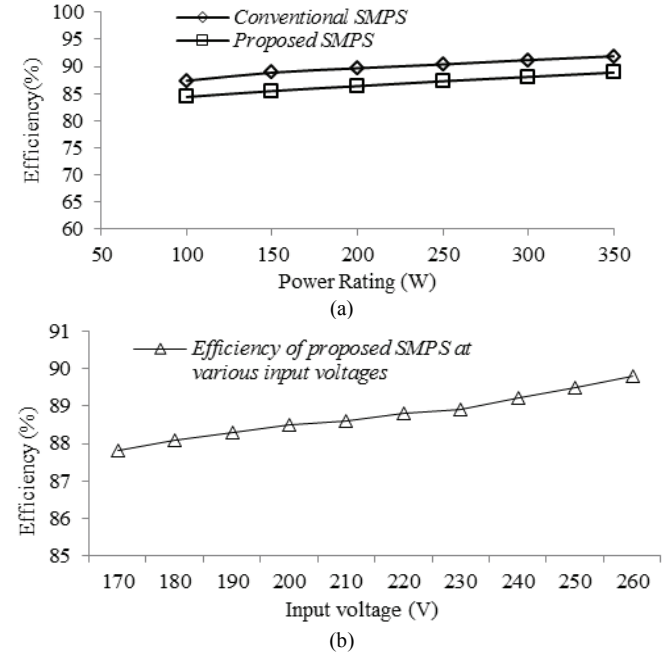


Fig.15. Efficiency of the proposed System (a) Variation in efficiency of SMPS at various loading conditions, (b) Variation in efficiency of SMPS at various input voltages

From these test results, it is clear that the proposed Zeta converter based SMPS system is capable of eliminating the power quality problems that are present in the conventional computer power supplies and is a recommendable solution for computers and other similar appliances.

VIII. Conclusion

A DCM operated front end PFC converter cascaded with a multiple output isolated converter has been used for the design of an SMPS for PCs. It has been designed, modeled, simulated and developed for input power quality improvement and output voltage regulation. All the dc output voltages are regulated by controlling only one output voltage. Three different modes of operation of the front end converter have been carried out in simulation to select the best possible operation especially based on device stresses. Finally, the best suited mode of operation for the front end converter has been implemented in an experimental prototype. Test results obtained from the prototype conform to the ones obtained via simulations. From the recorded test results, it is evident that the proposed power supply is able to mitigate power quality problems that are present in the conventional SMPS systems. Based on these results, it is concluded that the proposed SMPS configuration in PCs is expected to yield improved THD of ac mains current with almost unity PF under wide range of input voltages and loads.

Appendix

A. Design of Input Capacitor for Proposed Power Supply

The input capacitor is designed to reduce the 100 Hz ripple which is reflected from the single phase ac mains. The input power P_{in} for a single phase ac mains is expressed as [6],

$$P_{in} = V_m \sin\omega t * I_m \sin\omega t = V_{in} I_{in} (1 - \cos 2\omega t) \quad (14)$$

The second term is the reflected 100Hz ripple on the input capacitors of the half bridge VSI and is expressed as,

$$i_C(t) = -\frac{V_{in} I_{in}}{V_o} \cos 2\omega t \quad (15)$$

where, $i_c(t)$ is total current flowing in capacitors C_{h1} and C_{h2}. An output voltage ripple for given capacitors' current is as,

$$\Delta V_o = \frac{1}{C} \int i_C(t) dt = -\frac{I_o}{2\omega C} \sin 2\omega t \quad (16)$$

The value of sin(ωt) is considered 1 for the maximum voltage ripple at the capacitor. Therefore, it is rewritten as,

$$C = \frac{I_o}{2\omega \Delta V_o} \quad (17)$$

The capacitor is estimated for eliminating 100 Hz ripple as,

$$2C_{h1} = 2C_{h2} = \frac{I_o}{2\omega \Delta V_o} \quad (18)$$

The equal value input capacitors C_{h1} and C_{h2} are calculated as 0.6mF for a ω of 314 rad/sec, ΔV_o of 6V (2%) and an output current of 1.17A.

B. Design of Input Capacitor for Conventional Power Supply

The input voltage applied to the single phase diode bridge rectifier is given as,

$$v_{in} = V_m \sin(\omega_L t) \quad (19)$$

where V_m is the peak value of supply voltage and ω_L is the

fundamental frequency in rad/sec.

The input voltage appearing after the diode bridge is given as,

$$v_{in} = |V_m \sin(\omega t)| \quad (20)$$

where | | represents the modulus function. The average voltage (V_{in}) appearing across the diode bridge is calculated as $V_{in} = 2V_m/\pi$.

A diode bridge fed power supply requires a bulky capacitor which maintains a constant dc voltage at the input to isolated converter. This capacitor (C_{h1}=C_{h2}) is designed as,

$$2C_{h1} = 2C_{h2} = \frac{V_m}{2f_L R_L \Delta V_{dc}} \quad (21)$$

The output voltage ripple ΔV_{dc} is expressed as,

$$\Delta V_{dc} = \frac{V_m}{4f_L R_L C_{h1}} \quad (22)$$

The voltage ripple calculated is 9.39V which is higher than the one calculated for the proposed SMPS for the same value of capacitor.

REFERENCES

[1] Limits for Harmonic Current Emissions, International Electro technical Commission Standard, 61000-3-2, 2004.

[2] IEEE Recommended Practices and Requirements for Harmonics Control in Electric Power System, IEEE Standard 519, 1992.

[3] H. Aintablian, "The harmonic currents of commercial office buildings due to non-linear electronic equipment," in *IEEE Conf. SOUTHCON*, 1996, pp. 610-615.

[4] E. M. Gulachenski, and D. P. Symanski, "Distribution circuit power quality considerations for supply to large digital computer loads," *IEEE Trans. Power Apparatus and Systems*, vol. PAS-100, no. 12, pp. 4885-4892, 12 Dec. 1981.

[5] D. O. Koval, and C. Carter, "Power quality characteristics of computer loads," *IEEE Trans. Ind. Applications*, vol. 33, no. 3, pp. 613-621, 1997.

[6] N. Mohan, *Power Electronics: A First Course*, John Wiley and Sons Inc, USA, 2011.

[7] L. Umanand, Power Electronics Essentials & Applications, Wiley India Pvt. Ltd., 2012.

[8] Xueshan Liu, Jianping Xu, Zhangyong Chen and Nan Wan "Single-inductor dual output buck-boost power factor correction converter," *IEEE Trans. Ind. Electron.*, vol. 62, no.2, pp. 943-952, Feb. 2015.

[9] H.S. Athab, D.D.-C. Lu, A. Yazdani and Bin Wu,"An efficient single switch quasi active PFC converter with continuous input current and low dc bus voltage stress," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1735-1749, April 2014.

[10] Yi-Ping Su, Chia-Lung Ni, Chun-Yen Chen, Yi-Ting Chen, Jen-Chieh Tsai and Ke-Horng Chen, "Boundary conduction mode controlled power factor corrector with line voltage recovery and total harmonic distortion improvement techniques," *IEEE Trans. Ind. Electron.,* vol. 61, no. 7, pp. 3220-3231, July 2014.

[11] Hyoung-Suk Kim, Jae-Kuk Kim, Ki-Bum Park, Hyun-Wook Seong, Gun-Woo Moon and Myung-Joong Youn, "On/Off control of boost PFC converters to improve light-load efficiency in paralleled power supply units for servers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1235-1242, March 2014.

[12] M. A. Dalla Costa, J. M. A. Álvarez, J.Garcia, A. L. Kirsten and D. G. Vaquero, "Microcontroller-based high-power-factor electronic ballast to supply metal halide lamps," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1779-1788, April 2012.

[13] H. Wei, and I. Batarseh, "Comparison of basic converter topologies for power factor correction," in *IEEE Proc. Southeastcon'98*, April 1998, pp. 348-353.

[14] H.Y. Kanaan and K. Al-Haddad, "Design, study, modeling and control of a modified Sheppard Taylor PFC," in *IEEE Conf.* on *Ind. Electron*., 2009, pp.856-862.

[15] A. Peres, D. C. Martins and I. Barbi, "Zeta converter applied in power factor correction," in *IEEE Proc.* of *PESC'94*, 1994, pp. 1152-1157.

[16] B. Singh, B.N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.,* vol. 50, no. 5, pp. 962-981, Oct. 2003.

[17] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, "Comprehensive study of single-phase ac-dc power factor corrected converters with high-frequency isolation," *IEEE Trans. Ind. Informatics*, vol. 7, no. 4, pp. 540-556, Nov. 2011.

[18] J.M. Alonso, J. Viña, D.G. Vaquero, G. Martínez and R. Osorio, "Analysis and design of the integrated double buck-boost converter as a high-power-factor driver for power-LED lamps," *IEEE Trans. Ind. Electron.,* vol. 59, no. 4, pp.1689-1697, April 2012.

[19] B. Singh and V. Bist, "A BL-CSC converter fed BLDC motor drive with power factor correction," *IEEE Trans. Ind. Electron.,* vol.62, no.1, pp. 172-183, May 2014.

[20] C. Martins, G. N. de Abreu, "Application of the Zeta converter in switched-mode power supplies," in *IEEE Power Conversion Conf.'93*, April 1993, pp. 147-152.

[21] Eng. Vuthchhay, C. Bunlaksananusorn and H. Hirata, "Dynamic modeling and control of a Zeta converter," in *International Symposium* on *Communications and Information Technologies*, *ISCIT'08,* 2008, pp. 498-503.

[22] E. Niculescu, M. C. Niculescu, and D. M. Purcaru, "Modeling the PWM Zeta converter in discontinuous conduction mode," in *IEEE Proc*. of *MELECON*, 5-7 May 2008, pp. 651-657.

[23] B. Singh., B. P. Singh and S. Dwivedi, "AC-DC zeta converter for power quality improvement in direct torque controlled PMSM drive," *Journal of Power Electronics,* vol. 6, no. 2, April 2006.

[24] S. Singh and B. Singh, "Voltage controlled PFC zeta converter based PMBLDCM drive for an air-conditioner," in *IEEE Conf.* on *Industrial and Information Systems*, *ICIIS 2010*, Jul 29-Aug 01, 2010.

[25] D. S. L. Simonetti, J. Sebastián, and J. D. Uceda, "Control conditions to improve conducted EMI by switching frequency modulation of basic discontinuous PWM preregulators," in *IEEE Power Elect. Specialists Conf., PESC'94,* vol. 2, 1994, pp. 1180-1187.

[26] H. Mao, A. Qahouq, J. S. Luo and I. Batarseh, "Zero-voltage-switching half-bridge DC-DC converter with modified PWM control method," *IEEE Trans. Power Electronics*, vol. 19, no. 4, pp. 947-958, July 2004.

[27] C. J. Wu, F. C. Lee, S. Balachandran and H. L. Goin, "Design optimization for a half-bridge dc-dc converter," *IEEE Trans. Aerospace and Electronic Systems*, vol. AES-18, no. 4, pp. 497-508, July1982.

[28] Chien-Ming Wang "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 969-972, Feb. 2008.

[29] D. Czarkowski and M. K. Kazimierczuk, "Circuit models of PWM half-bridge DC-DC converter," in *35th Midwest Symposium on Circuits and Systems,* vol.1, 1992, pp. 469-472.

[30] MathWorks, Inc. Protected by U.S. patents ©1984-2012.

[31] V. Vlatkovic, D.Borojevic and F. C. Lee, "Input filter design for power factor correction circuits, *IEEE Trans. Power Electron.*, vol.11, no.1, pp. 199-205, January 2005.

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